VLBI Standard Hardware Interface Specification – VSI-H

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History and Acknowledgements

The incompatibility of various VLBI data systems has long been recognized as posing a serious obstacle to the realization of the full potential of VLBI observations. Sporadic efforts have developed over the years to define a common interface standard which would allow observations recorded on different VLBI data systems to be processed at a common correlator, but these efforts have foundered for various reasons.

The establishment of the Global VLBI Working Group (GVWG) in the early 1990's, growing primarily from the space-VLBI community but serving the broader interests of astronomy, and the International VLBI Service (IVS) in 1998, serving primarily the geodetic VLBI community, provided an organizational framework for which efforts at standardization could proceed in a more organized and sanctioned fashion. It was from these roots that the present effort was initiated.

The fledgling VSI concept leading to the current specification was first proposed at the time of the GEMSTONE meeting in Tokyo in January 1999 and was discussed by a small interested group at that meeting. Support was then sought and received from IVS and GVWG to create a VSI Technology Coordination Group (VSI-TCG) comprised of experts representing all of the major world institutions involved in the development of VLBI equipment. The members of this committee are Wayne Cannon (York University/Crestech, Canada), Brent Carlson (DRAO, Canada), Dick Ferris (ATNF, Australia), Dave Graham (MPI, Germany), Tetsuro Kondo (CRL, Japan), Nori Kawaguchi (NAO, Japan), Misha Popov (ASC, Russia), Sergei Pogrebenko (JIVE, Netherlands), Jon Romney (NRAO, U.S.), Ralph Spencer (Jodrell, England), Alan Whitney (Haystack, U.S., Chairman) and Rick Wietfeldt (JPL, U.S.).

Early in the discussions it was decided to separate the hardware and software VSI, concentrating first on hardware, hence this VSI-H specification, to be followed by a companion software specification, VSI-S. The VSI-H specification was shaped by intensive e-mail discussions, plus three (multi-hour!) international telephone conferences and a two-day international VSI meeting held at Haystack Observatory in February 2000.

The current VSI-H specification is intended as a starting point from which to progress, and will be extended and amended as requirements and technology demand. It is heartening that already at this writing at least three groups are known to be developing or adapting VLBI data systems to meet the VSI-H standard.

The VSI-H specification represents the work of many individuals at many institutions, even well beyond those named in the formal VSI-TCG. The chairman would like to particularly acknowledge the important contributions of Dick Ferris, Rick Wietfeldt, the entire Japanese group, and the Crestech group in this effort.

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16 July 2000

1. Introduction

This document defines a VLBI Hardware Standard Interface (VSI-H) to and from a VLBI 'Data Transmission System' (DTS) that allows heterogeneous DTS's to be interfaced to both data-acquisition system (DAS) and data-processing system (DPS) with a minimum of effort. The interface is defined to be compatible with traditional recording/playback systems, network data transmission and even direct-connect systems. It is designed to completely hide the detailed characteristics of the DTS and allow the data to be transferred from DAS to DPS in a transparent manner.

The VSI-H specification defines the notion of a 'channel quantum', which is the maximum data rate that can be carried on a single standard VSI-H data connector. The basic VSI-H specification specifies a 'channel quantum' of 1.024 Gbps on a single 80-pin connector, with extensions to 2.048 and 4.096 Gbps. Higher data rates may be realized simply by parallel use of two or more 'channel quanta'.

A VLBI Standard *Software* Standard Interface (VSI-S) to accompany VSI-H is proposed but does not yet exist.

2. Intent of the VSI-H Specification

The intent of the VSI-H specification is to define a standard electrical and timing interface, along with a control *philosophy*. In this sense, VSI-H is not intended to be completely 'plug and play', and will require at least some software customization in each case; the future adoption of a VSI-S specification will hopefully minimize the software customization as well. Nevertheless, the adoption of a standardized interface at the hardware level should help to relieve many of the existing incompatibilities that now exist between various VLBI data systems.

The VSI-H specification is primarily aimed at normal data-taking and data-correlation tasks commonplace to VLBI. However, note will also be made of other related activities such as translation of tape media (i.e. tape copying) and parallel operation of multiple DTS's.

3. Structure of the VSI-H Specification

The VSI-H specification is structured as a *base* specification plus a set of *optional extensions*. Adherence to the optional extensions is desirable but not mandatory.

4. Levels of Compliance

Full compliance with the VSI-H specification is expected for all *future* systems designed by parties agreeing to the VSI-H specification. Existing systems are expected to be modified to comply on a *best-effort* basis only. For the purpose of indicating the degree of compliance to the VSI-H standard, two levels of compliance are established:

Level A – Fully compliant with the base VSI-H specification

Level B – Compliant with the VSI-H base specification *except* for one or more of the following:

1. Support for fewer than 32 bit streams (Section 7)
2. Incomplete signal-switching or active-signal-selection capability (Section 9)
3. Incomplete support of full range of f_{CLOCK} (Section 10)
4. Incomplete delay-offset support (Section 8.4)

5. Lack of support for PDATA/QDATA and/or PVALID/QVALID signals (Sections 10 and 11)
6. Incomplete test-vector capability (Section 13)
7. Data-replacement format (Section 14)

Non-support of the optional extensions to 64 and 128 MHz does not affect VSI-H compliance.

5. Assumptions on which VSI-H Specification is Based

The VSI-H specification is based on the following set of assumptions:

- The DTS is fundamentally a receiver and transmitter of parallel *bit streams* between a Data-Acquisition System and a Data Processing System.
- The *meaning* of individual bit streams is not specified; normally, a bit-stream is a stream of sign or magnitude bits associated with particular samples, but the actual meaning is to be mutually agreed upon between the DAS and DPS.
- The received and transmitted bit-stream clock rates may be different (e.g. the playback rate into the DPS may be speeded-up or slowed-down), however all received bit-stream information rates on acquisition are the same, and all bit-stream clock rates on transmit are the same.
- A single time-tag applies to all parallel bit streams. The DAS time-tag of every bit in every bit-stream must be fully recoverable at the output of the DTS.

Note that, under these assumptions, no restrictions or specifications are placed on the type or format of the medium used to transport the data through the DTS; magnetic tape, disk, optical fiber, Internet or any other type of transmission medium is allowed.

6. Data Transmission System (DTS) Structure

For the purposes of the VSI-H specification, the DTS is divided into two logical modules, as indicated in Figure 1:

1. The 'Data Input Module' (DIM) is responsible for accepting multiple parallel bit streams, accompanied by a common clock and common 1-second tick, applying a common time-tag ('observe time'), and sending them to a *transmission medium* (tape, disc, fiber-optic, etc.).
2. The 'Data Output Module' (DOM) accepts data from the *transmission medium*, decodes the accompanying 'observe-time' information, and recreates the data-streams in accordance with an external clock and '1-second' tick.

The entire DTS (DIM plus DOM) may reside either in a single physical module or in separate physical DIM and DOM modules.

7. Data Input Module (DIM)

A simplified model of one 'channel quantum' of the Data Input Module is shown in Figure 1.

7.1 *DIM Interface*

7.1.1 Input signals from the DAS to the DIM–

1. BS_0 through BS_{31} – 32 parallel bit-streams, all sampled by the DIM at the same rate, which may be selected to be 2, 4, 8, 16 or 32 MHz,

corresponding to the 'bit-stream information rate' (f_{BSI}). The maximum aggregate DIM input data rate is 1.024 Gbps for one 'channel quantum'.

Any 1, 2, 4, 8, 16 or all 32 input channels may be selected and marked as 'active'. Only 'active' bit-streams are sampled and made available at the DOM output.

Optional extension of f_{CLOCK} to 64 and 128 MHz provides maximum aggregate rates of 2.048 and 4.096 Gbps, respectively.

2. CLOCK – a clock accompanying the bit-streams, also providing a reference frequency for the DIM, at 2, 4, 8, 16 or 32 MHz with optional extension to 64 or 128MHz. Note $f_{CLOCK} \geq f_{BSI}$.
3. 1PPS – a 1pps tick which defines the corresponding parallel data bits which are to be time-tagged on the integer second. The 1PPS signal is timed to coincide with the data bit taken on the second tick (the 'TOST' bit).
4. PVALID – signal that specifies the 'validity' of the BS_n bit streams. The content and use of the PVALID signal is not defined by the VSI-H specification.
5. A standard 8-bit ASCII asynchronous serial data stream, PDATA, which may send a burst of up to 2048 bytes of information between each 1PPS tick. The content and use of this information is not specified by the VSI-H specification.

7.1.2 DIM Control Interface

The DIM control interface is a 2-way communications interface, implemented in both RS-232 and Ethernet, and normally connected to a computer. The control interface both controls and monitors the operation of the DIM. The DIM controller must be aware of 1PPS ticks to the extent that certain critical messages can be reliably sent to the DIM between specific 1PPS pulses, and that certain messages can be reliably transmitted from the DIM between specific adjacent 1PPS pulses.

If the DIM and DOM reside in the same physical unit, they may share a single set of control interfaces.

7.1.3 Other Signals

1. ALT1PPS – an external (possibly asynchronous) signal which may be selected as a substitute for 1PPS, as indicated in Figure 1. An example of ALT1PPS might be the 1pps tick from a station atomic clock.
2. DOTMON – a monitor signal from the DIM which allows confirmation of the epoch of the DOT-clock second tick (see Section 7.2).

7.2 *The Data-Observe-Time (DOT) Clock*

As shown in Figure 1, the DIM maintains an internal Data-Observe-Time (DOT) clock which has the following properties:

1. The DOT clock is the master clock within the DIM, and is used to unambiguously mark each incoming data bit with its current reading to the full resolution of CLOCK.
2. The DOT clock may be set to a specified second of time (presumably UTC) on a given 1PPS or ALT1PPS tick.

3. Once set, the DOT clock keeps time solely by counting CLOCK cycles (i.e. subsequent 1PPS/ALT1PPS ticks are ignored by the DOT clock unless the DOT clock is expressly commanded to be reset).

7.3 *Example of DIM Operation*

The following is an example of a typical sequence of operations of a DIM in a normal observing situation:

1. Through the Control Interface, the DIM is configured to accept any particular subset of 1, 2, 4, 8, 16 or 32 of the incoming bit-streams, all at a specified bit-rate. Only these specified bit streams will be sampled by the DIM and relayed to the DOM.

2. Through the Control Interface, the DOT clock is commanded to be set to a specified integer second of time on the *next* 1PPS (or ALT1PPS) tick [see Note 6 below]. Once set, the DOT clock keeps time by counting cycles of CLOCK, ignoring subsequent 1PPS/ALT1PPS signals. The DOTMON monitor signal allows confirmation of the DOT epoch setting.

3. Through the Control Interface, the DIM is commanded to begin transmitting the selected input bit streams to the *transmission medium*. Each bit in each data stream must be transmitted with its accompanying time tag, either explicitly or implicitly.

4. At the end of the observing period, the DIM is commanded (through the Control Interface) to cease transmitting data.

Notes:

1. The method the DIM uses to record/transmit data or to time-tag data is irrelevant to the VSI-H specification.

2. Each type of DIM may have various control and configuration requirements which are outside the VSI-H specification.

3. It is the responsibility of the DAS to implement any multiplexing or de-multiplexing that may be necessary to transform sampled data into bit streams presented to the DIM. It is explicitly noted, however, that the DTS designer is free to implement any DTS-internal multiplexing scheme so long as the DOM output bit-streams are faithful reproductions of the DIM input bit-streams.

4. Some DIM systems may have the ability to transmit additional low-data-rate information, such as bit-stream identification and high-level global validity (i.e. ‘antenna on-source’), in addition to the bit-streams themselves. Such information may be transmitted to the DIM via the Control Interface or, in some cases, via the PDATA and/or PVALID data streams. The VSI-H specification neither requires nor prohibits any such capability.

5. With the exception of ALT1PPS, DOTMON and the Control Interface, all DIM interface signals are contained in a single 80-pin connector (see Section 12).

6. The Control Interface must be designed so that the controlling computer can, on request, be notified in a timely way of the occurrence of a 1PPS/ALT1PPS tick so that the control computer can unambiguously command the DIM to set the DOT clock to a specified integer second of time on the *next* 1PPS/ALT1PPS tick. The subsequent relationship between 1PPS/ALT1PPS and DOTMON can then be monitored either internally within the DIM [preferred] or externally to verify the 1PPS/ALT1PPS vs DOTMON relationship. In addition, the control computer should be able to verify the

DOT epoch by requesting that the DIM report the DOT setting at the occurrence of the *next* DOTMON tick.

8. Data Output Module (DOM)

A simplified model of the Data Output Module is shown in Figure 1.

8.1 *DOM Interface*

8.1.1 Input timing signals from the DPS –

1. A clock, DPSCLOCK, from the DPS which acts as a reference frequency for the DOM.
2. A '1-pps tick', DPS1PPS, which is used to set an internal DOM clock called the 'Requested Observe Time' (ROT) clock to an integer-second epoch in a manner similar to the way 1PPS sets the DOT clock in the DIM.

8.1.2 Output signals from the DOM to the DPS –

1. Reconstructed bit-streams, RBS_0 through RBS_{31} - accurate reproductions of the active sampled bit-streams transferred from the DIM except in so far as (i) they may be collectively speeded up or slowed down with respect to f_{BSI} at the input to the DIM, and (ii) switching within the DOM allows an arbitrary mapping of bit-streams to output signals RBS_0..RBS_{31}. The reconstructed bit streams are at a common rate called the 'reconstructed bit-stream information rate' (f_{RBSI}).
2. RCLOCK – the clock accompanying the reconstructed bit streams, at 2, 4, 8, 16 or 32 MHz with optional extension to 64 or 128 MHz. Note that $f_{RCLOCK} \geq f_{RBSI}$.
3. R1PPS – reconstructed 1PPS accompanying the bit streams, subject to the same speed-up or slow-down as RBS_n, but may be delayed by a specified amount with respected to ROT1PPS. The R1PPS tick *always* marks the data bit(s) corresponding to the 'TOST bit' at the DIM input.
4. ROT1PPS - 1pps tick from ROT clock, subject to the same speed-up or slow-down as the reconstructed bit streams.
5. QVALID – a 1-bit global signal indicating that the reconstructed data are judged by the DOM to be correct (i.e. tape is reproducing properly). May optionally be extended to include more sophisticated validity indications, such as pulsar gating, or as a pass-through of PVALID from the input to the DIM.
6. QDATA – A standard 8-bit ASCII serial data stream which may send a burst of up to 2048 bytes of information framed between each R1PPS or ROT1PPS tick (user can select to frame QDATA between either; see Section 14.2). The content and use of this information is not specified by the VSI-H specification.
7. Control Interface --The DOM control interface is a 2-way communications interface, encompassing *both* RS-232 and Ethernet, which both controls and monitors the operation of the DOM. The DOM controller must be aware of DPS1PPS to the extent that certain messages can be reliably sent to/from the DOM between specific adjacent DPS1PPS pulses. May be shared with DIM control interface.

8.1.3 Other Signals

ROTMON – a monitor signal from the DOM which allows confirmation of the epoch of the ROT-clock second tick (see Section 8.2).

8.2 *The Requested Observe Time (ROT) Clock*

The DOM maintains an internal Requested-Observe-Time (ROT) clock which maintains the reference time to which the re-constructed data are to be synchronized. The ROT clock has the following properties:

1. The ROT clock is set to a specified second of time on a given DPS1PPS tick.
2. Once set, the ROT clock keeps time solely by counting DPSCLOCK cycles (i.e. subsequent DPS1PPS ticks are ignored unless the ROT is expressly commanded to be reset). The monitor signal ROTMON allows confirmation of the ROT epoch setting.

8.3 *Speed-up/Slow-down Data Reproduction*

Some systems may also allow the DOM output bit rate (f_{RBSI}) to be speeded-up or slowed-down by certain factors compared to the DIM input rate (f_{BSI}). In such cases, the ROT-clock-increment per DPSCLOCK-cycle must be commanded to change correspondingly. The rates of RCLOCK, ROT1PPS, R1PPS and RBS_n will all change correspondingly.

The VSI-H specification does not mandate any speed-up or slow-down capability, nor does it constrain the implementation of such capability.

8.4 *Delay Offset*

In a *storage-based* DPS system, where the data are actually captured to a transportable storage medium and then replayed at a later time, a delay-offset capability in the DOM allows control of data alignment into the DPS. In these storage-based systems, VSI-H specifies that the DOM include the capability to offset the delay of the reconstructed bit-streams with respect to the ROT clock, as indicated in Figure 1. The delay is specified as a *bit offset.* This allows adjustment of the data delay into the DPS for processing. When the delay offset is set to a non-zero value, the RBS_n bit streams, R1PPS and QVALID[1] signals are delayed with respect to the ROT1PPS tick by the amount specified. When the delay offset is zero, ROT1PPS and R1PPS are coincident. QVALID indicates that valid data with the proper delay is being output from the DOM.

The range of the available delay offset in a *storage-based* DPS system shall be sufficient to cover at least ± 0.5*ROT1PPS. This allows an arbitrarily large offset (with respect to some DPS master clock) to be specified with a combination of ROT setting and bit offset.[2]

The design of the DOM should be such that the ROT clock and the delay offset can be set independently without disturbing the other.

In a *direct-transmission* DPS system, where the data are transmitted directly from DIM to DOM and not stored in a transportable medium, the required delay offsets are primarily a function of the geographic extent of the VLBI data-collection network. In this case, the

[1] That is to say that QVALID remains synchronized to the RBS_n bit streams to which it pertains.

[2] It has been pointed out that implementing a specified delay in the DIM between 1PPS and the DOT-generated 1pps may also provide some useful features, such as test-vector verification in some cases, or in compensating for a known epoch error in 1PPS or ALT1PPS. The implementation of such a delay capability in the DIM is optional and not part of the VSI-H specification.

DPS is assumed to implement the necessary data-delay requirements and VSI-H mandates no delay capability.

8.5 *Example of DOM Operation*

The following is an example of a typical sequence of operations of a DOM in a common data-playback situation:

1. Through the Control Interface, the DOM is configured to reproduce any desired subset of the 'active' bit streams sent to it by the DIM.

2. Through the Control interface, the ROT clock is commanded to be set to a specified UTC integer second of time on the *next* DPS1PPS tick; a delay offset may also be specified (see Section 8.4). Once set, the ROT clock keeps time by counting cycles of DPSCLOCK, ignoring subsequent DPS1PPS signals.

3. Through the Control Interface, the DOM is commanded to begin transmitting the selected input bit streams *synchronized to the ROT clock or specified bit offset from the ROT clock.* For tape-playback systems, this means the DOM must use a combination of mechanical tape positioning and electronic buffering to synchronize the recorded data to the ROT clock. When the output data are properly synchronized (with a delay offset, if any) and valid, the QVALID signal is asserted logical 'true'.

4. At the end of the data-period of interest, the DOM is commanded (through the Control Interface) to cease transmitting data.

Notes:

1. Note that the reconstructed data streams from the DOM are, except possibly for the data-stream clock rate and for playback errors or intentionally replaced data (see Section 14.1), identical to the data sampled by the DIM.

2. It is the responsibility of the DPS to do any manipulations necessary to transform the reconstructed bit streams into usable data (such as multiplexing or demultiplexing).

3. Some DOM's may have the ability to reproduce additional low-data-rate information transmitted from the DIM, such as bit-stream identification, etc. in addition to the bit-streams themselves. Such information may be accessed in the DOM via the Control Interface or, in some cases, transmitted via the QDATA serial-data stream. When performing a tape-copying operation, for example, QDATA may be used in conjunction with its DIM counterpart, PDATA, to transfer time-tag data to execute simple tape copying operations. The VSI-H specification does not mandate content or usage of QDATA.

4. Since the DPS is presumed to have some internal buffering, ROT1PPS and RCLOCK need not be precisely aligned with DPS1PPS and DPSCLOCK.

5. With the exception of DPS1PPS, DPSCLOCK, ROTMON and the Control Interface, all DOM interface signals are contained in a single 80-pin connector (see Section 12.1).

6. The procedure for setting and monitoring of the ROT clock is similar to that for the DOT clock in the DIM.

9. Signal Selection and Switching

9.1 *DIM*

As implied in the discussions above, the DIM must include the capability to select as 'active' any subset of 1, 2, 4, 8 or 16 of the 32 potential BS_n input data streams. Only the selected set of bit-streams is required to be transmitted to the DOM. This enables the DTS to more efficiently use the transmission medium in cases of reduced aggregate data rates.[3]

9.2 *DOM*

The DOM is required to reconstruct only the 'active' set of bit-streams transmitted to it by the DIM. However, the DOM must include the capability to connect *any* of the reconstructed bit-streams to any DOM RBS_n output bit-stream. Figure 1 shows a 32x32 crossbar switch as a functional illustration of this capability, but the designer is free to implement this specification in any satisfactory manner, including a separate external module (presumably containing its own control interface).

10. Signal Descriptions

10.1 *DIM Input Signals*

Signal	Frequency/Period	Voltage	Comments
CLOCK	f_{CLOCK} = 2, 4, 8, 16, 32 MHz with optional extensions to 64 and 128 MHz (see Table 2); Variability up to ±100 ppm	LVDS(see Section 12.1)	f_{CLOCK} sets maximum BS_n sample rate; variability to allow for high-velocity spacecraft applications
1PPS	1 per f_{CLOCK} cycles of CLOCK (e.g. 1 per $32x10^6$ CLOCK cycles for 32 MHz CLOCK	LVDS	Rising edge should be synchronous with rising edge of data bit to be tagged as 'taken on the second tick' (the 'TOST' bit); see Figure 2
ALT1PPS	Alternate 1PPS signal	LVDS	May be asynchronous with CLOCK
BS_n n=0 to 31	Sampled by DIM at 'bit-stream information rate' (f_{BSI}); $f_{BSI} \leq f_{CLOCK}$	LVDS	For all clock rates, TOST bit (see Section 11.1) must be coincident with 1PPS; one data bit accepted every 2^k CLOCK cycles thereafter
PDATA	115 kbaud 8-bit serial data; one stop bit, no parity	LVDS	Up to 2048 bytes to be received *between* each 1PPS tick

Table 1: DIM Input Signals

f_{CLOCK} [f_{RCLOCK}] (MHz)	f_{BSI} [f_{RBSI}] (Mbps)						
	2	**4**	**8**	**16**	**32**	**64**	**128**
2	Y						
4	Y	Y					
8	Y	Y	Y				
16	Y	Y	Y	Y			
32	Y	Y	Y	Y	Y		
64 (opt)	Z	Z	Z	Z	Z	Z	
128 (opt)	Z	Z	Z	Z	Z	Z	Z

Table 2: Required combinations of clock frequencies and internal bit-stream data rates

Table 2 notes:

1. 'opt' indicates optional
2. 'Y' indicates required. 'Z' indicates required if that optional clock frequency (or a higher one) is implemented.
3. Clock frequencies of 64 and 128 MHz are optional extensions to the VSI-H standard.

[3] A signal-switching capability at the DIM input may be useful to order the bit-streams so that the default DOM output bit-stream ordering is more directly compatible with a target DPS, but this capability is not required. See also footnote in Section 13.4

Notes:

1. Use of ALT1PPS is intended for systems where the station 1PPS coming from an independent external source such as a hydrogen maser. In such a case, the ALT1PPS cannot be guaranteed to be synchronous with CLOCK, which may result in a ±1 CLOCK cycle ambiguity in the setting of the DOT clock. This will normally be of little consequence so long as the DOT clock is not subsequently reset, which could cause a timing discontinuity.
2. Strictly speaking, the ALT1PPS signal need only be a single pulse to set the DOT clock, but is typically a repetitive signal at a 1-pps rate. Following the setting of the DOT clock, the DOTMON monitor signal generated by the DOT clock is a useful indicator of proper DOT-clock synchronization.
3. Each input bit-stream, BS_n, is sampled by the DIM only once every 2^k, k=0,1,2,… periods of CLOCK, where k is determined by the relevant cell value in Table 2. This sample rate is known as the 'bit-stream information rate' (f_{BSI}). This allows, for example, the DAS samplers to always run at f_{CLOCK}, even though f_{BSI} is lower than the DAS sample rate.
4. The inclusion of PDATA is primarily for future use, particularly for tape copying, where the output of a DOM can be connected directly to the input of a DIM. In such a case, the QDATA output from the DOM can dynamically transmit data time to the DIM to automatically update the DOT clock. Other uses of PDATA are also possible (see Section 14.2).
5. Any discontinuity or frequency change of CLOCK, other than the allowed variability of ±100 ppm, will normally require the DIM, including the DOT clock, to be reset.

10.2 *DIM Output Signals*

Signal	**Frequency/Period**	**Voltage**	**Comments**
DOTMON	Same as 1PPS	TTL	For monitor purposes only

Table 3: DIM Output Signals

Notes:

1. The DOTMON signal provides a useful monitor that indicates the DOT is properly synchronized to 1PPS/ALT1PPS.
2. The inclusion in the DIM of other useful monitor signals is encouraged.

10.3 *DOM Input Signals*

Signal	**Frequency/Period**	**Voltage**	**Comments**
DPSCLOCK	Allowed frequency is dependent on f_{RCLOCK}, as given in Table 5; Variability up to ±100 ppm	LVDS	Sets max f_{RBSI}; variability to allow for high-velocity spacecraft applications
DPS1PPS	1 per $f_{DPSCLOCK}$ cycles of DPSCLOCK (e.g. 1 per $32x10^6$ DPSCLOCK cycles for $f_{DPSCLOCK}$=32 MHz	LVDS	Sets epoch of ROT clock second tick

Table 4: DOM Input Signals

Notes:

1. The DPS1PPS signal is used only once to set the ROT clock epoch upon command, presumably at the beginning of a scan or tape.

2. Any discontinuity or frequency change in of DPSCLOCK, other than the allowed variability of ±100 ppm, will normally require the DOM, including the ROT clock, to be reset.

$f_{DPSCLOCK}$ (MHz)	f_{RCLOCK} (MHz)						
	2	**4**	**8**	**16**	**32**	**64**	**128**
2	Y						
4	Y	Y					
8	Y	Y	Y				
16	Y	Y	Y	Y			
32	Y	Y	Y	Y	Y		
64 (opt)	Z	Z	Z	Z	Z	Z	
128 (opt)	Z	Z	Z	Z	Z	Z	Z

Table 5: Required frequency combinations of DPSCLOCK and RCLOCK

Table 5 notes:

1. 'opt' indicates optional.
2. 'Y' indicates required. 'Z' indicates required if that optional clock frequency (or a higher one) is implemented.
3. CLOCK frequencies of 64 and 128 MHz are extensions to the VSI-H standard.

10.4 *DOM Output Signals*

Signal	**Frequency/Period**	**Voltage**	**Comments**
RCLOCK	f_{RCLOCK} is dependent on $f_{DPSCLOCK}$, according to Table 5	LVDS	Sets max output reconstructed bit-stream information rate (f_{RBSI})
R1PPS	1 pulse per second of ROT clock time	LVDS	May be 2^n (n=…-2,-1,0,1,2,...) R1PPS pulses per DPS1PPS, depending on DOM speedup factor (see Notes)
ROT1PPS	Same as R1PPS	LVDS	Coincident with R1PPS if delay=0 or delay option not implemented
RBS_n n=0 to 31	$f_{RBSI}=f_{RCLOCK}/2^k$, k=0,1,2,… in accordance with Table 2	LVDS	May be arbitrarily re-mapped
QVALID	Global logical indication that data is sync'ed and valid; no period	LVDS	
QDATA	115 kbaud 8-bit serial data; one stop bit, no parity	LVDS	Up to 2048 bytes transmitted *between* successive R1PPS or ROT1PPS ticks (selectable)
ROTMON	Same as ROT1PPS	TTL	For monitor purpose only

Table 6: DOM Output Signals

Notes:

1. Speed-up/slowdown on DOM playback is optional and may not be possible with all systems. No limits are placed on speed-up or slow-down factors.
2. If the DOM can operate with a speedup/slowdown, the ROT increment per DPSCLK must be specified to the DOM.

11. Signal Timing Relationships

11.1 *General*

Figure 2 shows the timing relationships between 1PPS, CLOCK and BS_n; timing relationships between R1PPS, RCLOCK and RBS_n are similar. The sample points for three different bit-stream information rates (f_{BSI}'s) are shown to illustrate that the epoch of the first sample taken after the rising edge of the 1PPS tick (the so-called 'TOST' sample) must maintain a constant timing relationship with respect to 1PPS regardless of the f_{CLOCK} or f_{BSI}. This guarantees that the epoch of the sampled data stream will not change with f_{CLOCK} or f_{BSI}. After the TOST sample, subsequent samples are taken every 2^k CLOCK cycles, depending on the ratio of f_{CLOCK} to f_{BSI}.

11.2 *Timing Ticks*

Table 7 specifies the minimum and maximum durations of various periodic ticks:

Signal	Type	Min duration	Max duration
1PPS	LVDS	1 cycle of CLOCK	500 ns (inverse 2 MHz)
ALT1PPS	LVDS	1 cycle of CLOCK	No specification
DPS1PPS	LVDS	1 cycle of DPSCLOCK	500 ns
R1PPS	LVDS	1 cycle of RCLOCK	500 ns
ROT1PPS	LVDS	1 cycle of RCLOCK	500 ns
DOTMON	TTL	Stretched for easy viewing	~10 ms
ROTMON	TTL	Stretched for easy viewing	~10 ms

Table 7: Timing-Tick Min/Max Durations

12. Interconnect Hardware Specifications

12.1 *LVDS Interfaces*

Three physical LVDS interfaces are present in the DTS:

1. DAS-to-DIM 'data interface' on an 80-pin MDR connector with 4-40 jackscrews; pinout specified in Table 8.
2. DOM-to-DPS 'data interface' on an 80-pin MDR connector with 4-40 jackscrews; pinout specified in Table 8. This pinout is compatible with the DAS-to-DIM connector to allow easy DOM-to-DIM connections.
3. 'Timing interface' on a 14-pin MDR connector with spring latch; pinout as specified in Table 9. If the DIM and DOM are separate physical units, each will have a 14-pin MDR connector.

The interfaces all conform to the LVDS differential format as defined by the ANSI/EIA/TIA-644 standard. All connectors are Mini D Ribbon (MDR) with sockets on both the transmitting and receiving equipment.

DAS-DIM	DOM-DPS	Pin(+)	Pin(-)	Comments
BS0	RBS0	1	2	
BS1	RBS1	3	4	
"	"	"	"	
"	"	"	"	
BS14	RBS14	29	30	
BS15	RBS15	31	32	
BS16	RBS16	42	41	
BS17	RBS17	44	43	

"	"	"	"	
"	"	"	"	
BS30	RBS30	70	69	
BS31	RBS31	72	71	
1PPS	R1PPS	33	34	
Unused	ROT1PPS	35	36	See 12.1.6 Notes
PVALID	QVALID	37	38	
CLOCK	RCLOCK	39	40	
PCTRL	QCTRL	74	73	Reverse-channel control: '1' (default) – forward only '0' – reverse permitted
PDATA	QDATA	76	75	
PSPARE1	QSPARE1	78	77	Spare signal 1
PSPARE2	QSPARE2	80	79	Spare signal 2

Table 8: MDR-80 Pin Allocations (Data Interface)

Signal	**Pin(+)**	**Pin(-)**
ALT1PPS	1	2
DPS1PPS	3	4
DPSCLOCK	5	6
Undefined (see 12.1.6 Notes)	7..14	

Table 9: MDR-14 Pin Allocations (Timing Interface)

12.1.1 Reverse Channel Control

Due to requirements of some system designers, the base VSI-H specification requires the use of only uni-directional signals in each of the two MDR connectors. In order to accommodate the *option* that some reverse-channel functions be allowed, three signal pairs (P/QCTRL, P/QSPARE1, P/QSPARE2) have been defined in the MDR-80 Data-Interface connector in Table 8:

P/QCTRL – a control signal asserted received by the DAS (as PCTRL) or transmitted by the DOM (as QCTRL) which specifies whether the two spare signal lines P/QSPARE1 and P/QSPARE2 are in the 'forward' or are allowed to communicate in the 'reverse' direction, as follows:

- P/QCTRL=1 (default state): no change, i.e. all signal channels transmit in the normal direction.
- P/QCTRL=0: Ports *optionally* fitted with transceivers for channels P/QSPARE1 and P/QSPARE2 will operate in the reverse direction, i.e. DPS to DOM or DIM to DAS. Thus static two signal 'back channel' or conventional half-duplex operation becomes possible.

Notes:

1. Equipment not installing the optional transceivers fix P/QCTRL in the default state and may continue to use P/QSPARE1/2 in the normal direction for any other "spare" purpose as desired.
2. Any combination of equipment with and without the optional transceivers may be connected without complication. Any combination with less than both optioned up, will by default operate in the normal (forward only) mode.

3. The reverse channels may only become active when explicitly commanded by the DAS or DOM. A disconnected cable automatically forces transceivers to the receive state.
4. LVDM (Multipoint) standard transceiver chips (e.g. SN65LVDM050/051) allow terminations at both ends of the line by driving double the normal current into it. Net waveform and timing specifications are indistinguishable from normal single-terminated LVDS.
5. No specific purpose is defined for the reverse channels, but see suggested usage below.

12.1.2 Suggested Reverse-Channel Usage

If the optional reverse channel capability described above is implemented, the PSPARE1/2 lines can carry the clocking signals normally assigned to the Timing Cable, integrating all 'reverse-channel' timing signal into the Data Cable and eliminating the need for the Timing Cable (though the MDR-14 connector must be present as well). Table 10 shows suggested signal assignments when P/QCTRL="0":

Signal	New Assignment	Direction	Comments
PSPARE1	TVGCTRL	From DIM	See Notes
PSPARE2	DOT1PPS	From DIM	See Notes
QSPARE1	DPSCLOCKX	To DOM	Substitute for DPSCLOCK
QSPARE2	DPS1PPSX	To DOM	Substitute for DPS1PPS

Table 10: Suggested Reverse-Channel Signal Assignments

Notes:

1. The use of QSPARE1/2 here are simply direct replacements for the signals DPSCLOCK and DPS1PPS.
2. The purpose of DOT1PPS is to allow a DAS otherwise without a 1-pps signal to receive DOT1PPS from the DIM via the Data Cable. This then enables the use of a TVG in the DAS (pseudo-random noise functions only) without requiring either a 1-pps input or a control port on the DAS. It also enable the periodic PDATA function which requires a 1-pps synchronizing signal.

12.1.3 Waveform Specifications

Figures 3 through 5, along with Table 11, specify the timing characteristics of the LVDS waveforms.

Parameter	Spec.	32MHz	64MHz	128MHz
T	$1/f_{CLOCK}$	31.3	15.6	7.8
t1	0.3T	9.4	4.7	2.3
t2	0.35T	10.9	5.5	2.7
t3	T-t1	21.9	10.9	5.5
t4	0.15T	4.7	2.3	1.2
t5	0.2T	6.3	3.1	1.6
t6	T-t4	26.6	13.3	6.6
t7,t8	$\geq$ 0.25	0.25	0.25	0.25
t7,t8	$\leq$ 0.2T	6.3	3.1	1.6

Table 11: LVDS Timing Specifications and Values (ns) at Rated Frequencies

12.1.4 Transmitter Specifications

1. The transmitter will produce waveforms satisfying the transmitter output eye pattern and transitions in Figures 3 and 5 when driving a standard LVDS receiver.
2. The default state of inactive signals is "1".
3. Pair to pair cross-talk : $\leq$-40dB

12.1.5 Receiver Specifications

1. Line termination (pair) : 100Ω ±5%.
2. Line receivers will fail-safe to a logical '1' state when disconnected.
3. The receiver will respond correctly to incident waveforms satisfying the receiver input eye pattern in Figure 4.

12.1.6 Cable Specifications

When driven by any transmitter conforming to the transmitter output eye pattern in Figure 3 the cable assembly will deliver waveforms satisfying the receiver input eye pattern in Figure 4, into a properly terminated receiver.

This formal specification is difficult to verify on such a wide interface so the following indirect specifications are offered as a guide:

1. Differential (odd-mode) characteristic impedance (pair) : 100Ω ±10%
2. Pair to pair skew : $\leq$ 0.1T
3. Rise time degradation : $\leq$ 0.1T
4. Attenuation : $\leq$ 9dB at f = 1/T
5. Pair to pair cross-talk : $\leq$ -40dB over 0.5/T < f < 5.5/T
6. Aggregate cross-talk : $\leq$ -30dB over 0.5/T < f < 5.5/T
7. Rated frequencies : 32MHz, 64MHz & 128MHz

Standard cable lengths are 5m, 10m and 20m.

Notes:

1. Cable assemblies comprise n-pair screened or 2n-line multi-coax cables, terminated by metal shrouded plugs which continue full screening through to the connection plane. Corresponding shrouds on the equipment connectors directly ground the shield to their respective chasses.
2. All input lines should be terminated normally even if a circuit is not implemented. This provides proper loads for all drivers and avoids problems due to resonances in floating wires in the cable.
3. MDR-80 only: 'Unused' signal on DIM connector pins 35-36 should be terminated normally as it will be driven by ROT1PPS when a DOM output is connected to a DIM input.
4. MDR-14 only: Ground undefined pins on receptacles. Connectivity within the cable not required. Grounding the spare pins reduces stray coupling on the board and within the connector. It also provides convenient returns for the drain wires from pair shields in some cable types. The enveloping cable shield is of course continuous with and returned to chassis, by the metal connector shrouds.

12.2 *TTL Interfaces*

The two monitor signals, DOTMON and ROTMON are the only TTL signals defined in the VSI-H specification. They are to 'back terminated' 50Ω ports, implemented by placing a ~50Ω resistor in series with the driver chip.[4] The rising edge of these signals is the active transition. Duration is to be stretched to be conveniently observed on an oscilloscope. The nominal time offset from 1PPS/ALT1PPS to DOTMON and from DPS1PPS to ROTMON should be provided to the user and is, ideally, independent of f_{CLOCK} (in the case of DOTMON) or $f_{DSPCLOCK}$ (in the case of ROTMON).

The DOTMON and ROTMON signals are to be carried on 50Ω BNC connectors.

12.3. *Control Interfaces*

The DIM and the DOM shall have *both* an Ethernet *and* an RS-232 control interface. Both may be simultaneously active, though this is not required. Some of the control and monitor functions, as discussed above, are quasi-real-time, in that control/monitor data must be reliably communicated between 1PPS pulses (in the DIM) or DPS1PPS pulses (in the DOM) in order to properly set and monitor the DOT and ROT clocks.

If the DIM and DOM are in the same physical unit, they may share the Ethernet and RS-232 control interfaces.

The details of the communications messages and protocols are to be specified in the VSI-S document.

Control Interface:

RS-232: DB-9 configured as DCE (pinout in Table 12)
Ethernet: RJ-45 jack (10Base-T or 10/100 Base-T)

Signal	Description	Direction	Pin	Comments
CD	Carrier Detect	From DTS	1	optional
RD	Received Data	From DTS	2	required
TD	Transmitted Data	To DTS	3	required
DTR	Data Terminal Ready	To DTS	4	optional
SG	Signal Ground	--	5	required
-	-	-	6	not used
RTS	Request to Send	To DTS	7	optional
CTS	Clear to Send	From DTS	8	optional
RI	Ring Indicator	From DTS	9	optional

Table 12: DB-9 Pin Allocations (EIA/TIA-574)

[4] This raises the output impedance of the driver chip to ~50Ω Given a 50Ω signal path all the way to the monitoring device (scope, for example), the forward wave is completely reflected by the high impedance of the monitoring device and absorbed back in the source.

The specifications of the control interfaces are:

1. RS-232: operating at least to 9600 baud, preferably higher (to 115 kbaud); 8-bit, 1 stop bit, no parity; software handshaking to be specified in VSI-S specification.
2. Ethernet: 10Base-T or 10/100Base-T

13. Test Vectors

Test-vector generators (TVG) and receivers (TVR) are used to validate the physical layer connections between the Data Acquisition System (DAS), Data Input Module (DIM), Data Output Module (DOM), and Data Processing System (DPS) components of the VLBI Data Transfer System (DTS).

The VSI-H specification imposes no requirements on testing the interface through the transmission medium from the DIM to the DOM, though designers are urged to implement testing procedures suitable to the characteristics of the DTS.

13.1 *General Characteristics*

The philosophy of the TV specification is to fully test the connection of user equipment to the DIM and DOM data interfaces. To this end, the TV system should have the following characteristics (see Figure 1):

1. The DIM includes a TVR to validate data transmission from equipment connected to the DIM data interface.
2. The DOM includes a TVG to validate data transmission from the DOM to external equipment.
3. Each TVG is capable of generating 32 unique pseudo-random noise (PRN) bit streams, denoted as TV_0-TV_{31}, each of a fixed period of 2^{15}-1 (32767) bits.
4. All PRN bit-streams are re-synchronized at each 1PPS/R1PPS epoch.
5. The TV bit-stream data rate is always at the rate of the data which it replaces. This implies that TV rates must be consistent with Table 2.

Though the VSI-H specification does not directly extend to the DAS or DTS, a complete TV system would also include a TVG in the DAS[5] and a TVR in the DTS.

13.2 *Test Vector Generator*

Figure 6 shows an example gate-level design of the TVG (based on Crestech design) to be used in VSI-H compliant DTS's. Each of the 32 output PNS bit-streams is re-initialized at each 1PPS/R1PPS tick. Table 13 tabulates the first 20-bits of each of the 32 TV bit-streams. Each bit stream has an approximate balance of the number of 'ones' and 'zeroes', corresponding to a 'DC-bias' of ~50%. Note that, for illustration purposes, the CLOCK signal in Figure 6 is shown to have the same frequency as the data-bit-stream sample rate.

In addition, each TVG must be capable of producing an "all 0's" or "all 1's" signal on all 32 bit-stream outputs. In this mode, it is useful to verify that the TVR's reports an error rate of ~50%.

[5] Including a TVG in the DAS probably only makes sense when the DIM receives and uses 1PPS from the DAS. The use of an asynchronous ALT1PPS makes the use of a DAS-TVG difficult.

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}	t_{16}	t_{17}	t_{18}	t_{19}	t_{20}
TV_0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
TV_1	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0	0
TV_2	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	0	0	0
TV_3	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0
TV_4	0	0	0	0	0	1	1	1	0	1	1	0	1	1	1	0	0	0	0	1
TV_5	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	0	0	0	0	1
TV_6	0	0	0	0	1	0	1	1	1	0	0	1	0	1	1	0	0	0	1	1
TV_7	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
TV_8	0	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	1	1	1
TV_9	0	0	0	1	0	1	0	0	0	0	1	0	1	0	1	0	0	1	1	1
TV_{10}	0	0	1	1	1	0	0	0	0	1	1	1	0	1	1	0	1	0	0	1
TV_{11}	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0
TV_{12}	0	1	1	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	0	0
TV_{13}	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
TV_{14}	1	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0
TV_{15}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
TV_{16}	1	1	1	1	1	1	1	0	1	1	1	0	1	0	1	1	1	1	1	1
TV_{17}	1	1	1	1	1	1	1	0	1	1	1	0	1	0	0	1	1	1	1	1
TV_{18}	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1	1
TV_{19}	1	1	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	1
TV_{20}	1	1	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1	1	0
TV_{21}	1	1	1	1	1	0	1	0	1	0	1	1	0	1	0	1	1	1	1	0
TV_{22}	1	1	1	1	0	1	0	0	0	1	1	0	1	0	0	1	1	1	0	0
TV_{23}	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
TV_{24}	1	1	1	0	1	0	0	1	1	1	0	1	0	0	0	1	1	0	0	0
TV_{25}	1	1	1	0	1	0	1	1	1	1	0	1	0	1	0	1	1	0	0	0
TV_{26}	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	1	1	0
TV_{27}	1	1	1	0	1	1	1	1	1	1	0	1	1	1	0	1	1	0	0	1
TV_{28}	1	0	0	1	1	1	1	1	0	0	1	1	0	0	0	0	1	0	1	1
TV_{29}	1	0	1	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1
TV_{30}	0	1	1	1	1	1	1	0	1	1	1	0	1	0	1	0	1	1	1	1
TV_{31}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1

Table 13: TVG data outputs for first 20 data bits following 1PPS/R1PPS

13.3 *Test Vector Timing Relationships*

As indicated in Figure 7, the TVG is initialized at every 1PPS/R1PPS tick in such a way that the 'TOST bit' at t_0 is undefined. From that point forward, the TVG increments every sample clock period and has the same timing relationship to CLOCK as normal user data. The TVG continuously cycles through the 32767-bit TVG sequence until the next 1PPS/R1PPS tick, at which point the TVG is again re-initialized.

13.4 *Test Vector Receiver*

On command, the DIM-TVR will measure and report the bit-error rate (BER) and "DC-bias" on each of the 32 input test bit-streams, either sequentially or simultaneously. In order to untangle possible bit-stream 'mix-ups' (i.e. bit streams being directed to the

wrong place), a useful, but not required, capability of the TVR is to examine each possible bit stream for each of the 32 possible TV sequences.[6]

The TVR reporting period may be selected to correspond to any integer number of 1PPS/R1PPS periods, up to a reasonable number (say ~64).

14. Other Notes and Comments:

14.1 *Data-Replacement Format*

Some systems may periodically replace small portions of data sampled by the DIM with timing and synchronization information. The use of a 'data-replacement' format under the VSI-H standard is allowed under Level B compliance. The QVALID signal must accurately flag any replacement data as 'invalid' as it emerges from the DOM. In addition, the use of standard VSI-H test-vector testing with the DAS and DPS may be difficult or impossible with a data-replacement format.

14.2 *Media Translation (Tape Copying)*

With the use of the VSI-H interfaces, data may be easily copied from one medium to another in a straightforward manner. The output of a DOM may be directly connected to the DIM input. For this purpose, the DOM must have the capability of 'standalone playback' without the connection of DPSCLK or DPS1PPS signals. In such case, the ROT clock will be commanded to simply track the playback time on the tape.

Time-tag transfer between DOM and DIM can be accomplished by two different methods. By using the DOM facility to transmit the ROT setting immediately following a R1PPS tick, a control computer can read the ROT and appropriately set the DOT clock in the DIM. Once ROT and DOT clocks are appropriately set, copying will take place with no further intervention until a time discontinuity (tape stop and restart, for example) when the DOT and ROT clocks must again be reset. Alternatively, time-tag transfer from DOM to DIM can be done through the QDATA/PDATA serial data lines (as discussed below).

14.3 *Usage of PDATA/QDATA*

The usage and content of the PDATA/QDATA asynchronous serial-ASCII signals is not specified under the VSI-H specification. A few possible uses of these signals are:

14.3.1 Media translation

During media-translation (i.e. tape copying) operations, where the DOM output is connected to the DIM input, QDATA may be used to transmit the high-level time (e.g. date and time to the unit-second level) to the PDATA input of the DIM between each R1PPS tick. In this case, it is probably most useful if the QDATA time tag corresponds to the epoch of the *next* R1PPS tick. This allows the DIM to dynamically set the DOT clock to the proper time at the next 1PPS (R1PPS) tick in much the same way the DOT clock is set in normal operation. Other auxiliary information may, of course, be transmitted between the DIM and DOM in the same way.

[6] It has been pointed out that placing a 32x32 crossbar switch in the DIM may aid in implementing this capability. In addition, the ability to route one selected data stream to a front-panel monitor connector could be of significant benefit in debugging difficult situations.

14.3.2 Auxiliary information from DAS

If the DAS is capable of supplying PDATA information to the DIM, this information may be used as the DIM sees fit. Possible information might include time, data-collection parameters, antenna pointing, system temperature, etc. If the system is capable, some or all of this information may be used to control the DIM, or perhaps transmitted to the DOM for output to QDATA.

14.3.3 Model parameters to DPS: An attractive possible use of QDATA is to periodically transmit station-model information to the DPS. This capability is particularly attractive if the DOM includes the capability to delay the data according to a dynamic model supplied to it by the host computer. If, for example, the ROT clocks of all DOM's are set to represent a center-of-earth clock and each DOM dynamically delays its output data according to a center-of-earth model, the DOM output data may be immediately available for correlation processing with only a small amount of FIFO re-synchronizing (using ROT1PPS tick) necessary in the DPS. The QDATA model parameters, transmitted between each ROT1PPS tick, would need only to carry such information as fractional bit delay, rate, plus a phase model for each channel, in order to provide the DPS with all necessary information to do proper processing.

14.4 *Usage of PVALID/QVALID*

The VSI-H specifies the use of the QVALID signal only to the extent that it indicates the global validity status of the DOM output data streams. If available to the DIM, the PVALID signal may be used to indicate that the DAS output data are 'valid'. This information can be used by the DIM as it sees fit, including transmitting it to the DOM for inclusion as a factor in controlling it QVALID output. If the DOM is sufficiently capable, the QVALID signal may also be used, for example, as a pulsar-gating mechanism to the DPS.

14.5 *Multiple Parallel DTS's*

In the event that a single DTS is not able to handle the required aggregate data rate, multiple DTS's may be employed in parallel. In the case of the DIM, the DAS must be able to support multiple DIM's in parallel, each being supported as if it were standalone. Multiple parallel DOM's can be handled in the same way.

14.6 *Multi-Port DTS*

A DTS may support multiple channel quanta simply by the inclusion of multiple MDR-80 data connectors on the DIM and DOM. Only a single MDR-14 connector for other timing signals is required. VSI-H imposes no requirements on signal connectivity between channel quanta within a multi-port DTS.

14.7 *Validity per Bit Stream*

Some DTS systems may benefit by having the capability to specify per-bit validity at the DOM output for each bit-stream individually. Currently the VSI-H specification says nothing about such a capability, but two possible options for such a capability have been discussed:

1. A parallel MDR-80 connector from the DOM can carry validity-per-bit-stream information. Depending on the resolution of the validity information, it may be necessary to also carry parallel timing information in the validity connector (RCLOCK, etc.). The pin-out of the validity connector would parallel that of the data connector.

2. Validity per bit stream can also be implemented without the addition of another connector by employing a 'bi-phase' code on each of the RBS_n output bit-streams. This works by using the second half of each RBS bit cell to indicate the validity state of that bit, so that the negative-going transition of RCLOCK samples the validity state of each bit cell of every RBS_n; this means that the effective RBS data rate is doubled. Coding is chosen so that a *change* of level in the second half of the bit cell signifies invalidation; this coding means that a bit stream without per-bit-validation is identical to a fully-valid bit stream with per-bit-validation. A DPS may choose to use this information or not. The 'bi-phase' scheme effectively doubles the information rate on the data connector, and as such may not be suitable for systems with clocking at 64 MHz or 128 MHz.

   The bi-phase coding scheme is common in commercial applications. Note that only *DOM-generated* signals are affected; these validity states are *not* transmitted from the DIM to DOM.

In either of these cases, the conditions used to control the per-bit-stream validation signals may presumably be specified by the user and are dependent on the details of the DTS system.

14.8 *Higher Clock Rates*

The possibility to move to bit-stream clock rates even higher than 128 MHz, particularly 256 MHz, is moving rapidly towards reality, particularly with introduction of extremely low-skew cable assemblies and higher-performance LVDS components. Though not currently a part of the VSI-H specification, this issue may well be ripe for re-examination in the future, and designers should keep the possibility in mind. At the appropriate time, it will be necessary to write the detailed specifications necessary to support these higher rates. Depending on high-speed-data technology developments over the next few years, it may also be advantageous to consider extending the VSI-H specification to include other well accepted data interfaces, such as high-speed serial links.

15. Glossary

15.1 *General*

BER	Bit Error Rate
'Channel Quantum'	The data carried on a single 80-pin LVDS signal connector; the base VSI-H specification defines a 'channel quantum' at a data rate of 1.024 Gbps.
DAS	Data Acquisition System; provides parallel bit-stream data to DIM
DIM	Data Input Module
DOM	Data Output Module
DOT	Data Observe Time; maintained in DIM
DPS	Data Processing System (most commonly a correlator)
DTS	Data Transmission System; includes DIM and DOM
f_{CLOCK}	Frequency of CLOCK signal
$f_{DPSCLOCK}$	Frequency of DPSCLOCK signal

f_{BSI}	Bit Stream Information Rate at input to DIM (i.e. DIM sample rate)
f_{RBSI}	Reconstructed bit-stream information rate at DOM output
LVDS	Low-Voltage Differential Signaling
ROT	Requested Observe Time; maintained in DOM
TOST bit	Data bit 'Taken On the Second Tick'; the TOST bit maintains a constant relationship to 1PPS and is always transmitted regardless of the bit-stream sample rate.
TV	Test Vector
TVG	Test Vector Generator
TVR	Test Vector Receiver
UTC	Universal Coordinated Time
VSI	VLBI Standard Interface
VSI-H	VSI Hardware Specification
VSI-S	VSI Software Specification

15.2 *Signals*

Name	Function	Format	Description
1PPS	DIM input	LVDS	One-second tick
ALT1PPS	DIM input	LVDS	Alternate one-second tick
BS_n	DIM input	LVDS	Bit-stream n
CLOCK	DIM input	LVDS	Data clock
DOT1PPS	DIM output	LVDS	Optional reverse-channel 1-pps from DOT clock (suggested use of PSPARE2)
DOTMON	DIM output	TTL	DOT clock 1-pps epoch monitor
DPS1PPS	DOM input	LVDS	DPS one-second tick to DOM
DPS1PPSX	DOM input	LVDS	Optional reverse-channel substitute for DPS1PPS (suggested use of QSPARE2)
DPSCLOCK	DOM input	LVDS	DPS clock to DOM
DPSCLOCKX	DOM input	LVDS	Optional reverse-channel substitute for DPSCLOCK (suggested use of QSPARE1)
PCTRL	DIM input	LVDS	Reverse-channel enable/disable
PDATA	DIM input	LVDS	115 kbaud asynchronous 8-bit data; up to 2048 bytes per 1PPS 'tick'; content unspecified by VSI-H
PSPARE1	DIM input/output	LVDS	Spare; optional use as reverse channel
PSPARE2	DIM input/output	LVDS	Spare; optional use as reverse channel
PVALID	DIM input	LVDS	Global 'data-valid'
QCTRL	DOM output	LVDS	Reverse-channel enable/disable
QDATA	DOM output	LVDS	115 kbaud asynchronous 8-bit data; up to 2048 bytes transmitted between 1PPS or ROT1PPS 'ticks'
QSPARE1	DOM input/output	LVDS	Spare; optional use as reverse channel
QSPARE2	DOM input/output	LVDS	Spare; optional use as reverse channel
QVALID	DOM output	LVDS	Global 'data valid'
R1PPS	DOM output	LVDS	'Reconstructed' 1PPS

RBSn	DOM output	LVDS	'Reconstructed' bit-stream n
RCLOCK	DOM output	LVDS	'Reconstructed' data clock
ROT1PPS	DOM output	LVDS	ROT clock 1-pps
ROTMON	DOM output	TTL	ROT clock monitor
TVGCTRL	DIM output	LVDS	Optional reverse-channel TVG control (suggested use of PSPARE1)

16. References

3M Connectors:

http://www.mmm.com/Interconnects/prod_con_0531.html

3M Pleated Foil Cable Assemblies:

http://www.mmm.com/Interconnects/Prod_cas_0804.html

Gore Max-Band Cable Assemblies:

http://www.gore.com/electronics/pages/cable/highdata/maxband.htm

TI LVDS Devices:

http://www.ti.com/sc/docs/schome.html

(At this site, perform "SC Parameter Search" for 'LVDS')

National Semiconductor LVDS Information

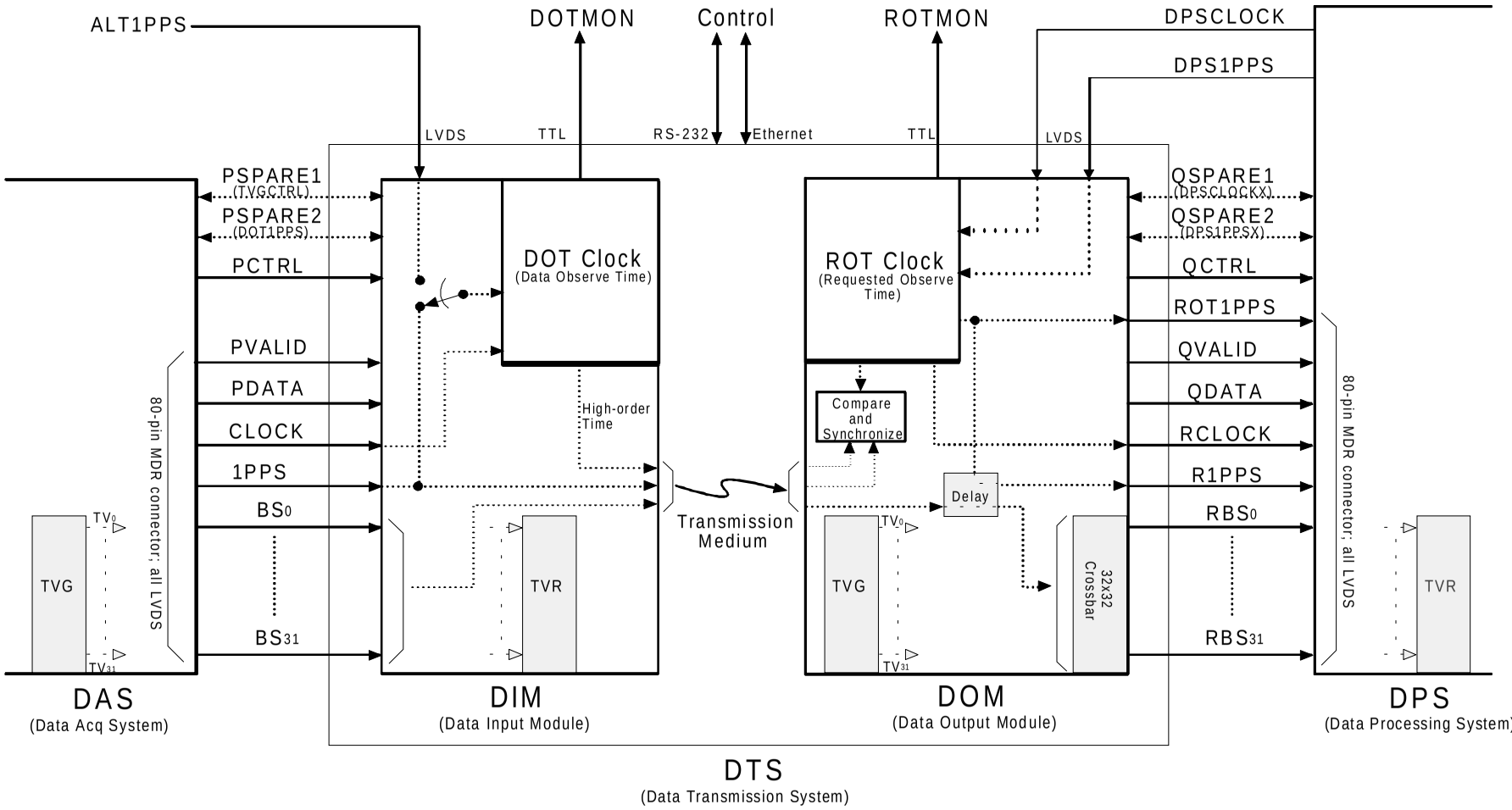
http://www.national.com/appinfo/lvds

(At this site, you can find the application notes by number or by category.)

Useful discussions of VSI interconnect issues:

VSI Interconnect Hardware Specifications, Dick Ferris, 15 March 2000

Derivation of Hardware Specs, Dick Ferris, 15 March 2000



Notes:
1. Shaded items are for illustrative purposes only.
2. PVALID is optionally transmitted from DIM to DOM.
3. PDATA is optionally transmitted from DIM to DOM.
4. Data delay in DOM is required only for storage-based systems.
5. See text for discussion of use of optional use of P/QSPARE1/2 signals.
6. If DIM/DOM in single box, ALT1PPS/DPSCLOCK/DPS1PPS share single MDR-14 connector.
7. This diagram does not show all functions and options -- see VSI-H specification for details.

FIG1.DRW
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Figure 1: VSI-H Functional Block Diagram

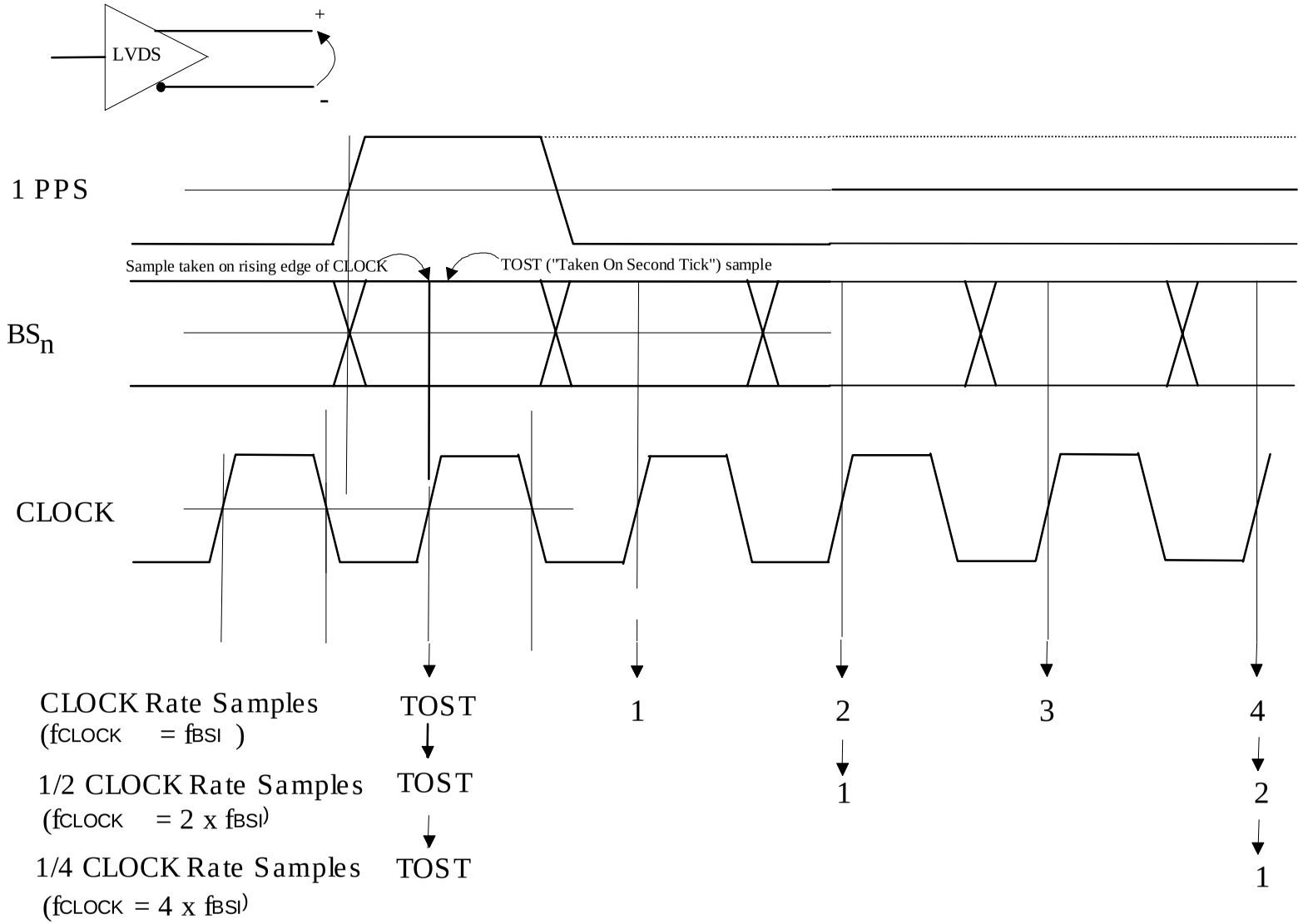


Figure 2: LVDS Timing Relationships

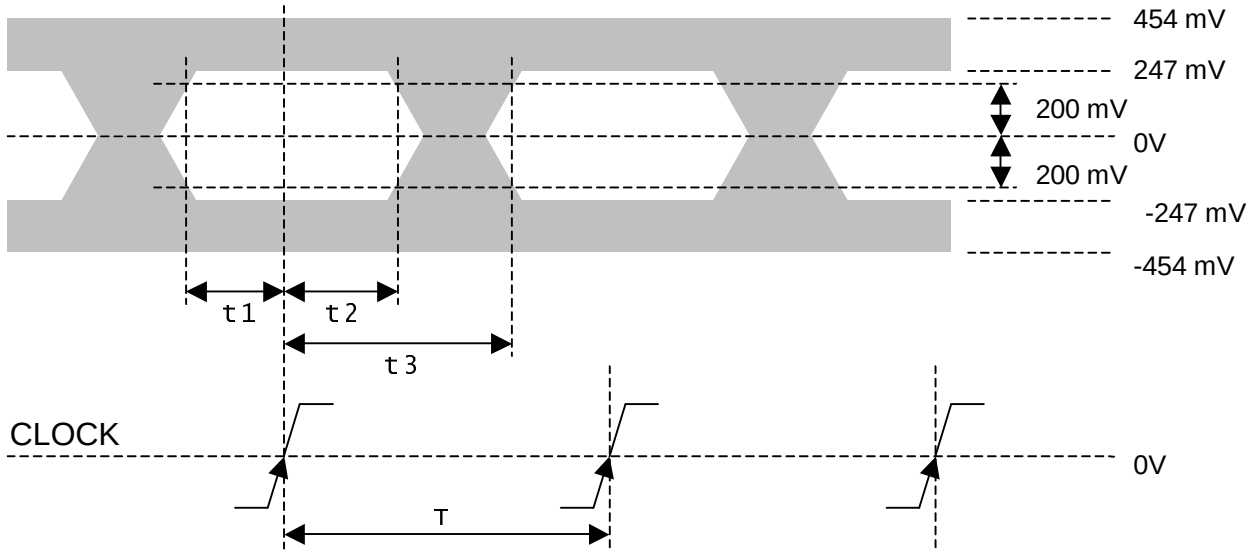


Figure 3: LVDS Transmitter Output Eye Pattern

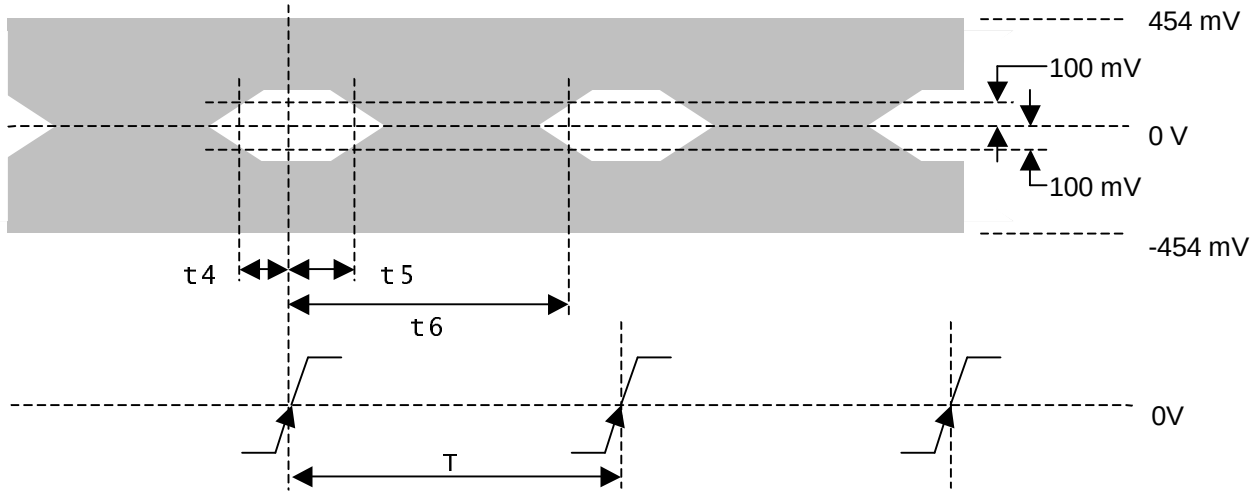


Figure 4: LVDS Receiver Input Eye Pattern

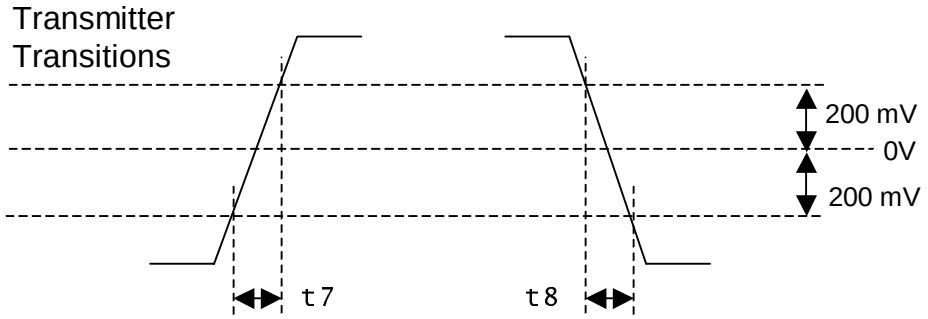


Figure 5: LVDS Waveform Transition Definitions

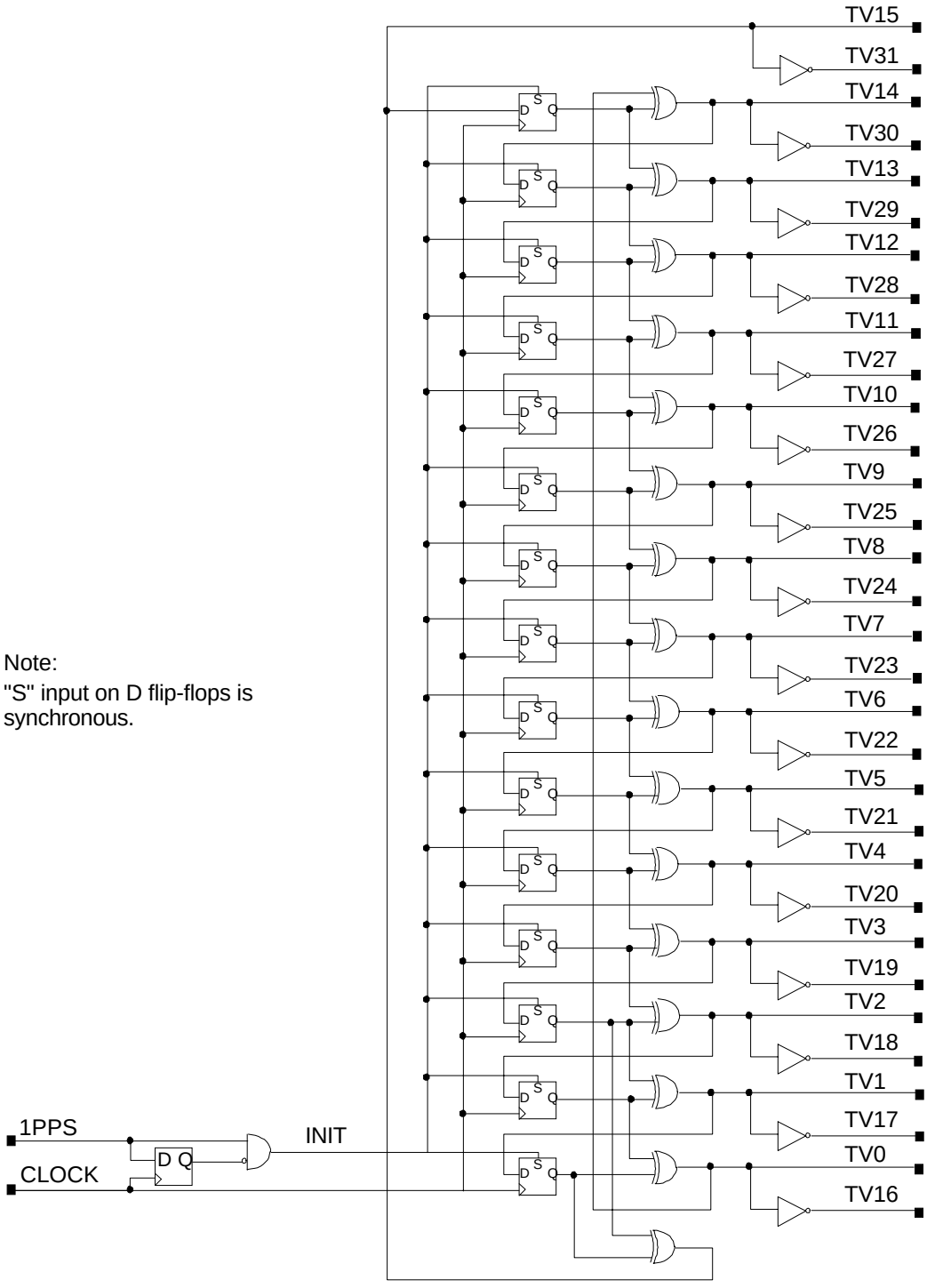
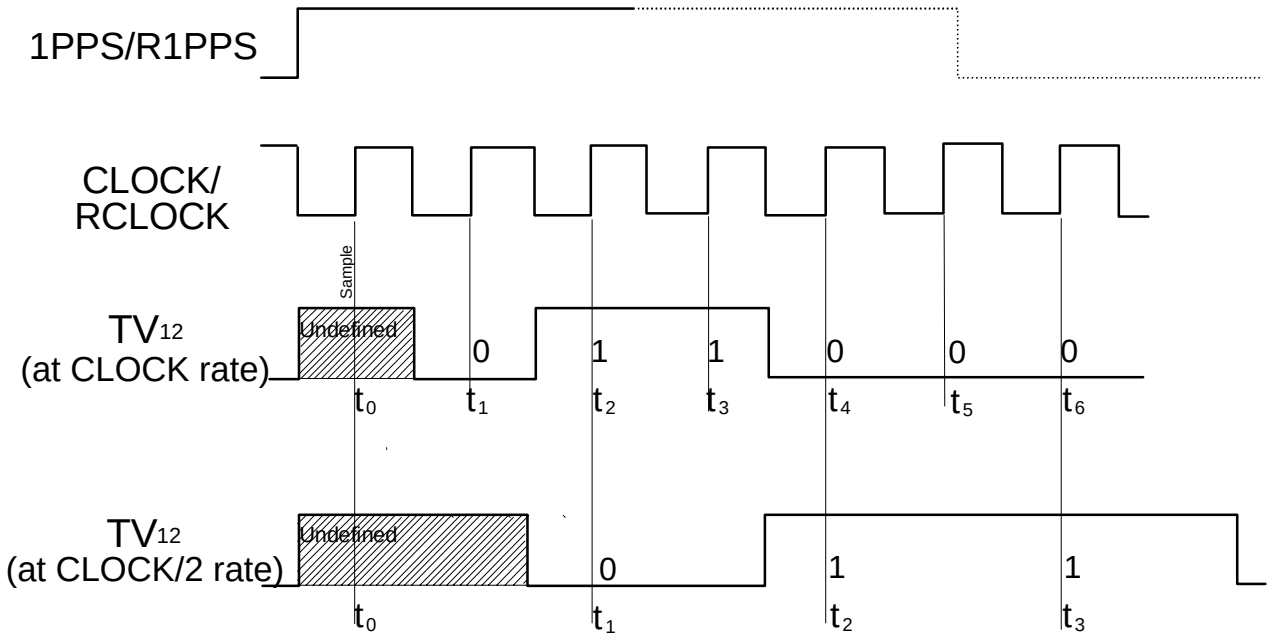


Figure 6: Test-Vector Generator Schematic

TVGEN.DRW
000422



Notes:

1. TV12 bit stream is shown for illustration.
2. The TV data streams have exactly the same timing relationship to CLOCK/RCLOC and 1PPS/R1PPS as actual data streams.
3. The TVG is initialized on every 1PPS/R1PPS tick. The TV value at t0 is undefined.
4. Starting with t1, the TVG continuously cycles through the 32767-bit TVG sequence until the next 1 PPS/R1PPS tick, at which point the TVG is again re-initialized.

Figure 7: TVG Timing Relationships

Appendix A: Revision History

Revision 1.0, 16 July 2000

First issue