Comments on 9th Feb Draft

Dick Ferris 31/3/00

1. Proposed Amendments

Item (1a)

Clarify section 4. *item* 3 *with* new text,

4. Levels of Compliance

.....

Level B – Compliant with the VSI-H base spec except for one or more of the following:

1. Support for fewer than 32 bit streams
2. Incomplete signal-switching or active-signal-selection capability
3. Incomplete support of all CLOCK frequencies ≤ 32MHz

Non support of the optional extensions 64 and 128MHz is not intended to affect compliance

Item (1b)

Include bit-stream selection of 'active' channels in DIM definition. also introduce BSCR *and* BSIR *and define the range of* CLOCK. *See* new text *in* 7.1. *vis:*

7.1 *DIM Interface*

1. Input signals from the DAS to the DIM–

a) 32 parallel bit-streams, BS_0 through BS_{31}, all at the same clock rate (BSCR), which may be sampled by the DIM at user-selectable rates of 2, 4, 8, 16 or 32MHz, the internal bit-stream information rate (BSIR). ~~Mbps/bit-stream for a~~ The maximum aggregate DIM input data rate ~~of~~ is 1.024 Gbps for one 'quantum channel'.

Any 1,2,4,8,16 or all 32 input channels may be selected in any order, and marked as 'active'. Only active bit-streams are sampled and transferred by the DIM to the DOM.

Optional extension t~~o rates~~ of BSCR and BSIR to 64 and 128MHz ~~Mbps/bit-stream~~ provides maximum aggregate rates of 2.048 and 4.096 Gbps, respectively.

b) ~~A~~ CLOCK – a clock accompanying the bit-streams, also providing a reference frequency for the DIM, at 2, 4, 8, 16 or 32MHz with optional extension to 64 or 128MHz. Frequency must be ≥ BSCR and ≥ BSIR.

The net effect of these changes, with formatting consistent with **8.1** *DOM Interface, is:*

7.1 *DIM Interface*

Input signals from the DAS to the DIM–

1. 32 parallel bit-streams, BS_0 through BS_{31}, all at the same clock rate (BSCR), which may be sampled by the DIM at user-selectable rates of 2, 4, 8, 16 or 32MHz, the internal bit-stream information rate (BSIR). The maximum aggregate DIM input data rate is 1.024 Gbps for one 'quantum channel'.

Any 1, 2, 4, 8, 16 or all 32 input channels may be selected in any order, and marked as 'active'. Only active bit-streams are sampled and transferred by the DIM to the DOM.

Optional extension of BSCR and BSIR to 64 and 128MHz provides maximum aggregate rates of 2.048 and 4.096 Gbps, respectively.

2. CLOCK – a clock accompanying the bit-streams, also providing a reference frequency for the DIM, at 2, 4, 8, 16 or 32MHz with optional extension to 64 or 128MHz. Frequency must be ≥ BSCR and ≥ BSIR.
3. 1PPS – a 1pps tick which defines the corresponding parallel data bits which are to be time-tagged on the integer second. The 1PPS signal is timed to coincide with the data bit taken on the second tick (TOST).
4. A PVALID signal that specifies the 'validity' of the BSn bit streams. Content and use of the PVALID signal is not defined by the VSI-H specification.
5. A standard 8-bit ASCII asynchronous serial data stream, PDATA, which may send a burst of up to 2048 bytes of information between each 1PPS tick. The content and use of this information is not specified by the VSI-H specification.

DIM Control Interface

The DIM control interface is a 2-way communications interface, implemented in both RS-423 and Ethernet, and normally connected to a computer. The control interface both controls and monitors the operation of the DIM. The DIM controller must be aware of 1PPS ticks to the extent that certain critical messages can be reliably sent to the DIM between specific 1PPS pulses, and that certain messages can be reliably transmitted from the DIM between specific adjacent 1PPS pulses.

Other I/O Signals

1. ALT1PPS – an external, possibly asynchronous, substitute for 1PPS.
2. DOTMON – a monitor signal for the one second tick of the internal DOT Clock (see following section).

Channel selection is significant functionality and deserves to be described up front. It complements the output distribution mechanism (crossbar) defined in the corresponding DOM definition.

BSCR and BSIR were introduced at the Haystack workshop but haven't previously found their way into the Draft.

Item (1c)

The names Dot1pps *and* Rot1pps *are inconsistent in format with all others in the document, and failure to appreciate the distinction (beyond an apparent typing inconsistency) between* Rot1pps *and* ROT1PPS *created great confusion for this reader. They also appear to have confused the author of the Draft in Section* 8.4>Notes>5. *Suggested new names are* DOTMON *and* ROTMON. *Replace in 14 and 10 places respectively.*

Item (1d)

This section has not evolved well with the Standard, and has become self-contradictory.

8.1 *DOM Interface*

.....

Output signals from the DOM to the DPS –

1. Reconstructed bit streams, RBS_0 thru RBS_{31}, accompanied by a common re-constructed clock (RCLOCK) and 1-pps (R1PPS). With the exception that the RBSn and R1PPS signals may be speeded up or slowed down relative to the rate at which they entered the DIM, they are identical reproductions of those entering the DIM. The maximum number of reconstructed bit streams corresponds to the number transmitted by the DIM (1, 2, 4, 8, 16 or 32); signal switching within the DOM allows an arbitrary mapping of bit streams to the actual DOM outputs RBS_0 to RBS_{31}.

The following is proposed:

Output signals from the DOM to the DPS –

1. Reconstructed bit-streams, RBS_0 through RBS_{31} - accurate reproductions of the active bit-streams transferred from the DIM except in so far as (i) they may be collectively speeded up or slowed down with respect to BSIR, their original rate, and (ii) switching within the DOM allows an arbitrary mapping of bit-streams to output signals RBS_0..RBS_{31}. The reconstructed bit-stream information rate (RBSIR) and clock rate (RBSCR) are always the same.

References to RCLOCK and R1PPS in the original para 1. above were superfluous given the presence of paras 2. *and* 4. *These latter require* extensions *as follows:*

2. RCLOCK – clock accompanying the bit-streams, at 2, 4, 8, 16 or 32MHz with optional extension to 64 or 128MHz. Frequency must be ≥ RBSIR.

4. R1PPS – reconstructed 1PPS accompanying the bit-streams, subject to the same speed up or slow down as the RBSn.

Item (1e)

Clarify issue of re-ordering bit-streams in the DIM.

9.1 *DIM*

As implied in the discussions above, the DIM must include the capability to select as 'active' and re-order, any ~~subset of~~ 1, 2, 4, 8, ~~or~~ 16 ~~of the~~ or 32 potential BSn input data streams. Only the selected set of bit-streams is required to be transmitted to the DOM. This enables the DTS to more efficiently use the transmission media in cases of reduced ~~aggregrate~~ aggregate data rates.

Item (1f)

In Table 2 *change the second primary heading to:*

BSIR
[RBSIR]
(Mbps)

and the caption to:

Table 2: ~~Allowed~~ Required combinations of clock frequencies and internal bit-stream data rates

and Table 2 notes: 3. *to:*

3. Clock frequencies of 64 and 128MHz are optional extensions to VSI-H.

As it stands, a table captioned "Allowed" contains entries designated "required" in fields indexed as "optional". This incongruity may be resolved by
(1) the first change in the caption (above)
(2) replacing the "Y"*s in the optional rows by* "Z"*s, and*
(3) adding to Table 2 notes: 1 *thus:*

1. 'Y' indicates required, 'Z' indicates required if that optional clock frequency (or a higher one) is implemented.

The notes: *would then read more logically if* 1. *and* 2. *were swapped.*

Item (1g)

While Table 2 *deals with the required relationships between BSIR and* f_{CLOCK}, Note 3. *covers the relationship between BSCR and the other two. Complete the description thus:*

10.1 *DIM Input Signals*
.....
Notes:
.....
3. Each input bit-stream, BSn, is sampled by the DIM only once every ~~CLOCK/2^k~~ 2^k, k=0,1,2,.. periods of CLOCK, where k is set by the operating point in Table 2. This allows, for example, the DAS samplers to always run at f_{CLOCK}, even though the data bit-streams are sampled at a lower rate by the DIM.

In general BSIR = BSCR/2^m, m=0, ±1, ±2,... where m>0 implies deliberate data decimation as in the example above, and m<0 would only occur when the input data is over sampled because its bit rate is below the supported range of BSIR.

Thus the CLOCK frequency, BSCR and BSIR are independent variables, except that neither BSCR nor BSIR may exceed f_{CLOCK}.

Item (1h)

In Table 1*, the* BSn *entry for* **Frequency/Period***:*

Allowed sample rates dependent on CLOCK frequency according to Table 2

is misdirected since Table 2 *deals with BSIR, applicable to internal signals, rather than BSCR which describes the input bit-streams. The appropriate entry is*

BSCR=$f_{CLOCK}/2^k$, k=0,1,2,...

Item (1i)

Table 5 is very similar to Table 2 and invites similar attention. vis:

Change Table 2 notes: 3. *to:*

3. Clock frequencies of 64 and 128MHz are optional extensions to VSI-H.

As it stands, a table captioned "Allowed" contains entries designated "required" in fields indexed as "optional". This incongruity may be resolved by
(1) the changing the caption:

Table 5: ~~Allowed~~ Required frequency combinations of DPSCLOCK and RCLOCK

(2) replacing the "Y"*s in the optional rows by* "Z"*s, and*
(3) adding to Table 5 notes: 1 *thus:*

1. 'Y' indicates required, 'Z' indicates required if that optional clock frequency or a higher one is implemented.

The notes: *would then read more logically if* 1. *and* 2. *were swapped.*

Item (1j)

Table 6 **Comments** *for* R1PPS:

May be 1, 2, 4, 8 or 16 R1PPS pulses per DPS1PPS, depending on DOM speed up factor

Is it necessary, or even wise, to imply a limit to the optional DOM speed up factor? eg. a flash disk DTS feeding 2Msps data into a 128MHz correlator. ..And then there's also 'slow down'..

Item (1k)

10.4 *DOM Output Signals*

.....

Notes:

.....

3. The DOM must include the functionality to map any reproduced bit-stream to any of the RBSn outputs. This is illustrated in Figure 1 as a 32x32 crossbar switch just prior to the output of the DOM, but the desired functionality can be achieved in other ways. Note that the addition of an external 32x32 crossbar switch between the DOM output and the DPS input will also create the required functionality.

The external crossbar concept hides a subtlety not necessarily apparent when it was proposed, namely, the DOM control structure, and implicitly VSI-S, is based on a single control interface. Therefore the external crossbar must be controlled directly from the DOM, or a meta-controller built into the extXbar to extract its commands from the control message stream. Similarly when a DIM employs deferred bit-stream remapping the DOM must merge the input and output mapping instructions and be able to transfer the resultant configuration to the extXbar in a transparent manner. Again this is easier if the extXbar is controlled directly from the DOM.

Item (1l)

10.5 *Validity per bit-stream (proposed extension)*

Some DTS systems may benefit by having the capability to specify per-bit validity at the DOM output for each bit-stream individually. This can be accomplished with no additional hardware by employing a 'bi-phase' code on each of the RBSn output bit-streams.

.....

The bi-phase coding scheme is quite common in commercial applications. .....

There are a couple of common biphase schemes, perhaps the best known is "Manchester" encoding. These are used frequently, but for the explicit purpose of embedding clock

information in a serial data stream. This is not relevant to our interface which is structurally orthogonal, with one of the most aggressive parallel structures extant.

*What is actually proposed here is the interleaving of two separate bit-streams. To decode them requires a double-frequency clock with rising edges ¼ period either side of the normal CLOCK transition, and to generate this requires logic running at 4*f_{CLOCK}, ie 512MHz, for our fastest interface. The associated MUX and DMUX circuits will run at 2*f_{CLOCK}.*

Furthermore, a DPS with such an interface will not be compatible with a non-extended DOM compliant at the same CLOCK rate, as its eye patterns need not be open at the ¼ T and ¾ T points. The DPS would have to support an ordinary interface as well.

Given the technological strictures of building a large high-speed parallel interface, the introduction of a double-rate bit-stream will halve the useful lengths of any cable type, and halve the operating frequency of any interface technology. In all we are looking at significant extra hardware, a factor of two loss of bandwidth, and a rather messy extension to the interface.

We aver that if per-bit and per-bit-stream VALIDITY is required it would be much easier and cheaper to provide a second standard interface in tandem, as previously proposed.

This does not appear to be an appropriate official extension to VSI

Item (1m)

11.4 *TTL*

The two monitor signals, Dot1pps and Rot1pps are the only TTL signals defined in the VSI-H specification; both are to be designed to drive into 50-ohms. The rising edge of these signals is the active transition. Duration is to be stretched to be conveniently observed on an oscilloscope. .....

If the only purpose of these signals is to drive a 'scope occasionally via coax, then a simpler scheme is to provide back-terminated 50Ω ports, by raising the output impedance of the driver chips with a series 43 or 47Ω resistor. Given a 50Ω signal path all the way, the forward wave is completely reflected by the normally high 'scope input impedance, and absorbed back in the source. The 'scope sees a full amplitude signal and there is no need to mess around arranging 50Ω terminations. The load on the driver chip is halved so that any contemporary CMOS gate can drive the line with a good waveform. This technique was used to good effect in the monitor ports of the CITF2 and I1 series MkII formatters.

Item (1n)

11.3 *LVDS*, **12.1** *DIM through* **12.6** *LVDS Device Standards, including* Tables 10, 11 *&* 12 *and footnote 2.*

1n.1 80-Pin Data Port

Alternative descriptions have been proposed in Item (4a) and discussed in Item (4b) below.

1n.2 14-Pin Auxiliary Port

Through an oversight this port was not referenced in Item (4a) and Item (4b). It carries the same type of signals as the data port and obviously it, and its associated cables, should perform to the same specifications.

Similar considerations apply to the connector pin allocations. Table 11: MDR-14 Pinout *becomes:*

Signal	Pin(+)	Pin(-)
ALT1PPS	1	2
DPS1PPS	3	4
DPSCLOCK	5	6
GND*	7..14	

Table 1 Auxiliary Port MDR-14 Pinout

* Ground unused pins on receptacles. Connectivity within the cable not required.

This pinout provides reduced cross-coupling and impedance discontinuity, especially with through-hole connectors (n.b. suitable surface mount types are available in this size). See Item (4b) for more details. It also puts all the active pins on the front row for easy routing.

Grounding the spare pins reduces stray coupling on the board and within the connector. It also provides convenient returns for the drain wires from pair shields in some cable types. The enveloping cable shield is of course continuous with and returned to chassis, by the metal connector shrouds.

1n.3 8-Pin Control Port

As it stands the signal specs are 'RS-423' (currently EIA/TIA-423-B) terminating on an 'RJ-45' (MJ8) connector.

RS-423 comprises single-ended 'RS-232' (EIA/TIA-232-F) compatible drivers and differential, explicitly 'RS-422' (TIA/EIA-422-B), receivers, over balanced lines. This implies a special interface box will be required by most if not all computers.

The pinout in Table 12 *is not part of -423 nor any other formal standard known to us, though it is used by well known Cisco Systems Inc. It has the unfortunate property that if a stock modular cable is used to join the interface to the DTS as implied in the text, the bizarre T568A/B wiring convention which pairs 3&6 and 4&5 together in the cable, will cause heaps of cross-coupling between the TD and RD signals.*

While there are other recognised pin allocations for balanced lines on MJ8s, we've strayed away from the original intention of providing direct and simple connections to the RS-232 based asynchronous serial ports commonly found on computers.

Enter EIA/TIA-561, an MJ8 DCE interface used in contemporary line modems in place of the cumbersome DB-25 RS-232 interface. It's electrical specs are -232 (strictly speaking EIA/TIA-562, a higher rate but otherwise equivalent standard) as are the control signal protocols if required. Not surprisingly COTS adaptors and patch cables for the common RS-232 (DB-25) and EIA/TIA-574 (DB-9) computer ports are available.

vis:

Computer (DTE)				DTS (DCE)	
T/EIA-232	T/EIA-574			T/EIA-561	
DB-25	**DB-9**	**Signal**	**Direction**	**MJ8**	**Comment**
22	9	RI	←	1	optional
8	1	DCD	←	2	optional
20	4	DTR	→	3	optional
7	5	SG	--	4	required
3	2	RD	←	5	required
2	3	TD	→	6	required
5	8	CTS	←	7	optional
4	7	RTS	→	8	optional

Table 2 Control Port, Computer to DTS Connections

While the Haystack meeting preferred to adopt the MJ8 (⇒ T/EIA-561) interface, there seems to be no practical reason why the -232 and -574 interfaces should not be allowed as (possibly equal) alternatives. Obviously DCE status and XON/XOFF flow control would be maintained. DTS support for RTS/CTS flow control may also be useful in some circumstances (but need not be mandated).

1n.4 LVDS Characteristics

Sections 12.3 *through* 2.6 *are variously covered in* *Item (4a)*.

Item (1o)

Clarify TV operating frequency:

> 14.1 *General Characteristics*
> .....
> 5. The TV bit-stream data rate is always f_{CLOCK}. ~~at the rate of the data which it replaces. This implies that TV rates must be consistent with Table 2.~~

There are 3 potentially different interface frequencies to consider on the DAS-DIM interface, namely f_{CLOCK}, BSCR and BSIR. We reason as follows:

BSIR: This is the DIM internal data rate; the DAS may be a fixed rate source and doesn't know about BSIR, so that sometimes BSCR>BSIR. Anyway testing of circuits operating at BSIR is an internal matter for the DIM.

BSCR: This is the data toggle rate on the physical interface and appears to be the 'natural' frequency for the TVG to substitute bit-streams. However the DIM may register the receiver outputs at f_{CLOCK} and then subsample at BSIR without otherwise needing to know about BSCR.

f_{CLOCK}: This is not only the most exacting frequency to check the interface, but it is actually CLOCK that is responsible for the waveform timing, and it is only because the bit-stream data may be constant for 2T, 4T, 8T, ... that intermediate transitions are missing so the net rate becomes BSCR<f_{CLOCK}. CLOCK is of course always present at both ends of the interface, so f_{CLOCK} is both the easiest as well as most appropriate frequency to use.

Item (1p)

14.1 *General Characteristics, footnote 3:*

> Including a TVG in the DAS probably only makes sense when the DIM receives and uses 1PPS from the DAS. The use of an asynchronous ALT1PPS makes the use of a DAS-TVG difficult.

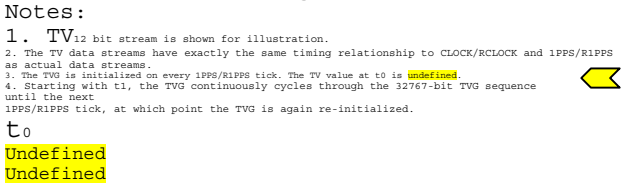
The inclusion of a TVG circuit in the DAS actually provides the means to inject the ALT1PPS signal into the system. Synchronisation to the next CLOCK edge is easy, and after that the TVG can use it and it gets passed on to the DIM as 1PPS in the normal way, to provide all 1PPS functions.

Item (1q)

14.3 *Test Vector Timing Relationships*

As indicated in Figure 4, the TVG is initialized at every 1PPS/R1PPS tick in such a way that the 'TOST bit' at t0 is undefined. .....

Figure 4: TVG Timing Relationships



When the TVG is reset its state is clearly 00..011..1, not "undefined" as stated (4 places). Why not label it "RESET" where necessary and leave it at that.?

Item (1r)

14.4 *Test Vector Receiver*

..... In order to untangle possible bit-stream 'mix-ups' (i.e. bit streams being directed to the wrong place), the TVR must be able to examine each possible bit stream for each of the 32 possible TV sequences. .....

This feature first appears in the 29 Jan. Draft but it's not evident in the VSI correspondence what its actual origin is, or the motivation behind it.

*It implies the need for a 32*32 correlator, a significant piece of hardware. It would have no role in the ordinary testing of interfaces, since there is no mechanism for bit-stream 'mix-ups' to occur. It may have a place while developing new systems (probably over-kill since the first 15 bits of each sequence are unique and easily resolved by inspection), but then that's not a qualification for VSI.*

I suggest that it be omitted.

Item (1s)

Following Item (1r) above it seems necessary to explicitly specify the position of TVG and TVR in their host systems. At the moment section 14*:*

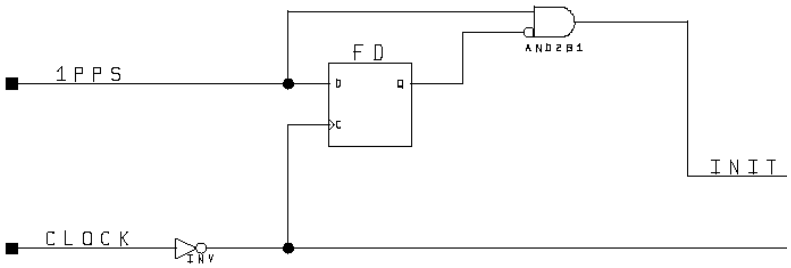
> **14. Test Vectors**
>
> Test-vector generators (TVG) and receivers (TVR) are used to validate the physical layer connections .....

is fairly clear as to their purpose and implies they connect directly to the line drivers and receivers respectively. In contrast Figure 1: VSI- H Functional Block Diagram *is at best equivocal about the relative position of the DIM TVR and the DIM input selector/ sampler/ mapper functions, and the DOM diagram clearly implies the TVG works* ***through*** *the output crossbar.*

Direct connection to the physical interface is clearly the intended configuration. The DIM and DOM data switches etc. are part of the internal data path and their operation should be validated as such. We note that the preponderance of common circuitry in the VSI TVG and TVR, and their position right on the external ports, make them an excellent basis for an internal validation system.

Item (1t)

`Figure 3 VSI TVG` *has acquired a control circuit:*



Since 1PPS is by definition already synchronous with CLOCK, the introduction of an inverter into the clock line as shown creates a timing race. While the intention is clear this is not appropriate for an engineering standard!

Given that in a real design both formatting the 1PPS/INIT pulse, and generating correctly phased bit-streams and CLOCK, will most likely happen elsewhere it is preferable to just stick to defining the logical process of generating the PRNs. e.g. Return to showing the sequence generator controlled by RESET (1Hz) and CK plus a supporting waveform diagram in the manner of the original CRESTech drawing. The design engineer can then incorporate this function and resolve the relationships with VSI specific waveforms in an appropriate manner.

2. Proposed New Items

Item (2a)

Insert a list of the optional extensions *after*

4. Levels of Compliance

The o-e*'s have been introduced in* 3. *We need a list somewhere so the reader doesn't have to hunt through the text for them. Given* 3 *and* 4 *this is as good a place as any. So far ∃ 6:*

*Interface operation at 64MHz (***7.1***)*
*Interface operation at 64 and 128MHz (***7.1***)*
*Delay offset (***8.3***)*
*Playback speed up, slow down (***5., 8.1, 8.2, 10.4***)*
*Validity per-bit (in some form or other) (***10.5***)*
Reverse Channels (proposed) (2c.1 below)

Item (2b)

Clarify DTS capacity requirements. Insert new section 10 *and (bump up all following).*

> **10. DTS Data Capacity**
> The total data transfer capacity between DIM and DOM is an implementation issue not constrained by this Standard. In practice it may be less than the aggregate capacity of the DIM or DOM interfaces.

Item (2c)

2c.1 Reverse Channels Function

This is a proposed new feature of the basic VSI definition. It defines the function of P/QCTRL, one of the 3 remaining spare signals on the 80-pin Data Port, but of itself requires no change to hardware or software.

The three spares are named for this purpose P/QCTRL (xConTRoL), P/QSPC (xSPare-C) and P/QSPD (xSPare-D).

P/QCTRL=1 (default state) ⇒ no change, ie all signal channels transmit in the normal direction.

P/QCTRL=0 ⇒ Ports ***optionally*** *fitted with transceivers for channels P/QSPC and P/QSPD will operate in the reverse direction, i.e. DPS to DOM or DIM to DAS. Thus static two signal 'back channel' or conventional half-duplex operation becomes possible.*

Notes:

1. Equipment not installing the optional transceivers fix P/QCTRL in the default state and may continue to use P/QSPC/D in the normal direction for any other "spare" purpose as desired.

2. Any combination of equipment with and without the optional transceivers may be connected without complication. Any combination with less than both optioned up, will by default operate in the normal (forward only) mode.

3. The reverse channels may only become active when explicitly commanded by the DAS or DOM. A disconnected cable automatically forces transceivers to the receive state.

4. LVDM (Multipoint) standard transceiver chips(e.g. SN65LVDM050/051) allow terminations at both ends of the line by driving double the normal current into it. Net waveform and timing specifications are indistinguishable from normal single-terminated '644 LVDS.

5. No specific purpose is defined for the reverse channels.

2c.2 Integrated DPS Clock Signals

This is a proposed ***optional extension*** *to VSI. Given the Reverse Channels Function 2c.1 it allows most DOMs to operate without the VSI Auxiliary Cable by placing ALTDPSCLOCK and ALTDPS1PPS on the DOM Data Cable. vis:*

ALTDPSCLOCK ⇔ QSPC; ALTDPS1PPS ⇔ QSPD

DOMs adopting this optional extension might use the internal QCTRL signal to automatically multiplex the ALT signals for the normal DPS signals on the Aux connector.

2c.3 Integrated ALT1PPS Signal

*This is a proposed **optional extension** to VSI. Given the Reverse Channels Function 2c.1 it allows a DAS otherwise without a 1pps signal to receive ALT1PPS from the DIM via the Data cable. This then enables the use of a TVG in the DAS (PRN functions only), without requiring either a 1pps input or a control port on the DAS. It also enables the periodic PDATA function which requires a 1pps synchronising signal.*

TVGCTRL ⇔ PSPC; ALT1PPS ⇔ PSPD

TVGCTRL=1 (default state) ⇒ normal bit-stream data; TVGCTRL=0 ⇒ TVG data.

Notes:

1. *TVG/normal operation is ultimately under control of the DAS and failsafe.*
2. *ALT1PPS will necessarily become synchronised in the TVG circuit, and may be sent back to the DIM as normal 1PPS.*

Item (2d)

Proposal for P/QDATA format

2d.1 Header

The first byte of each 2048 frame packet is a number 1..255 identifying the sending port. In each installation a unique address may be assigned to each transmitting VSI port.

Address = 0 ⇔ undefined.

This very simple 'packet header' serves to identify the contents in the normal way, and provides the CID or PID functions previously proposed. Since the xDATA channel is an information (c.f. bit-stream) link, the information is easily entered and recovered from the packets.

2d.2 Syntax

For general data we might consider the simple ASCII string syntax defined in standard IEEE 1284, vis

<key1>:<value>[,<value>];<key2>:<value>[,<value>];....

where the keys are all capitals (to aid readability when displayed) and the only special characters are the delimiters ":", "," and ";". No constraint is placed on the semantics of the value list.

e.g. *TIME:<yyyy>,<DOY>,<hh>,<mm>,<ss>;*
TIME:<mm>,<ss>;
TIME:+,<ss>;

In this example the TIME (set clock) function has been defined to accept full or partial value lists (right justified), and relative values.

3. Editorial Changes

(Typos, formatting etc not affecting substance of the standard. Format: ~~old text~~, new text)

Item (3a)

In section 5,

5. Assumptions on which VSI-H Specification is Based

.....

 The received and transmitted bit-stream clock rates may be different (e.g. the playback rate into the DPS may be speeded-up or slowed-down), however all bit-stream clock rates on acquisition must be the same, and all bit-stream clock rates on ~~transmit~~ transmission must be the same.

Item (3b)

Section **7.1** DIM Interface *has distinctly different formatting and style to its isomorph* **8.1** DOM Interface *(and different to the rest of the doc too). This tends to obscure the deliberate similarities between them. A compatible rendition of* **7.1** *is presented in Item (1b) above, incorporating current suggested changes.*

Item (3c)

7.3 *Example of DIM Operation*

.....

Notes:

1. The method the DIM uses to record/transmit data or to time-tag data is irrelevant to the VSI-H specification.
2. Each type of DIM may have various control and configuration ~~requirements~~ facilities ~~which are~~ additional to and outside the VSI-H specification.

Item (3d)

8.1 *DOM Interface*

.....

Output signals from the DOM to the DPS –

.....

7. Control Interface --The DOM control interface is a 2-way communications interface, encompassing both RS-423 and Ethernet, which both controls and monitors the operation of the DOM. The DOM controller must be aware of DPS1PPS to the extent that certain messages can be reliably sent to/from the DOM between specific adjacent DPS1PPS pulses.

Misplaced amongst the DOM-DPS signals, these deserve their own para. vis:

DOM Control Interface –

The DOM control interface is a 2-way communications interface, encompassing both RS-423 and Ethernet, which both controls and monitors the operation of the DOM. The DOM controller must be aware of DPS1PPS to the extent that certain messages can be reliably sent to/from the DOM between specific adjacent DPS1PPS pulses.

Immediately following the above introduce ROTMON (see Item (1c)), so far overlooked in this interface description:

Other DOM Signals –

ROTMON – external monitor of the ROT Clock setting, tied to R1PPS.

Item (3e)

Inserts in two places:

8.2 *The Requested Observe Time (ROT) Clock*

.....

3. Some DOM~~'~~s may allow the output data rate to be sped up/slowed down by a factor of 2^n . In such a case, the ROT-clock-increment per DPSCLOCK-cycle must be commanded to correspondingly increase. The rate of the R1PPS will correspondingly increase/decrease.

Item (3f)

Edits in three places:

8.4 *Example of DOM Operation*

.....

3. Through the Control Interface, the DOM is commanded to begin transmitting the selected input bit-streams *synchronized to the ROT clock or specified time offset (if delay option ~~if~~ is implemented) from the ROT clock.* For tape-playback systems, this means the DOM must use a combination of mechanical tape positioning and electronic buffering to synchronize the recorded data to the ROT clock. When the output data are properly synchronized and valid, the ~~PVALID~~ QVALID signal is asserted logical 'true'

.....

Notes:

1. ~~Note that the~~ The reconstructed data streams from the DOM are, except possibly for the.....

Item (3g)

Table 1 *has not cleanly broken over the page. To make it automatically flow across page boundaries (presumably it has not been manually split) do the following:*

First check that the paragraph formatting parameter "keep with next" is set in headings **10.** *and* **10.1** *(it normally is in the default heading styles).*

Then highlight the first column (only) of the table, ie from "Signal" to "PDATA" inclusive, by clicking above the table, or dragging a cursor down it. Format menu, choose "paragraph" and check "keep with next". From now on if a page break tries to interfere with the table, or separate it from its headings or caption, the whole lot will move onto the next page.

This is generally good practice with all headings and tables. There are other tricks to make headings repeat when very long tables have to break over more than one page.

Item (3h)

Most Table captions and associated Notes appear to be in ~8-point fonts compared with ~10-point main text. To our eyes it is preferable to use the same size. Indented formatting as shown is sufficient to distinguish the Notes.

Item (3i)

After Table 2, BSIR *subheadings* **64** *and* **128** *add* **(opt)**

Item (3j)

After Table 5, RCLOCK *subheadings* **64** *and* **128** *add* **(opt)**

Item (3k)

Table 6

VALID *should be* QVALID

Item (3l)

4 edits:

> **11.1** General
>
> Figure 2 shows the timing relationships between 1PPS, CLOCK and BSn; timing relationships between R1PPS, RCLOCK and RBSn are similar. ~~Two~~ Three different ~~clock~~ BSIR frequencies are shown to illustrate that the epoch of the first sample taken after the rising edge of the 1PPS tick (the so-called 'TOST' sample) must maintain a constant timing relationship with respect to 1PPS regardless of the CLOCK frequency BSCR or BSIR. This guarantees that the epoch of the sampled data stream will not change with clock frequency or sample rate. After the TOST sample, subsequent samples are taken every 2 k CLOCK cycles, depending on the ratio of CLOCK frequency to ~~sample rate~~ BSCR.

Item (3m)

If 1n.3 is adopted then numerous occurrences throughout the text of "RS-423" should change to "RS-232". Even though the actual standard has changed its name, this moniker carries with it the (technically wrong) presumption of asynchronous bit-serial transmission, and the various connector types and signal characteristics we are all used to.

Item (3n)

> **15.1** *Data-Replacement Format*
>
> Some systems may periodically replace small portions of data sampled by the DIM with timing and synchronization information. The use of a 'data-replacement' format under the VSI-H standard is allowed but not encouraged, and such systems would be granted only Level B compliance status. The QVALID signal must accurately flag any replacement data as 'invalid' as it emerges from the DOM. In addition, the use of standard VSI-H test-vector testing ~~with the~~ from DAS ~~and~~ through DPS may be difficult or impossible with a data-replacement format.

Normal interface testing DAS-DIM and DIM-DPS, (or DAS-DPS,) is not effected.

Item (3o)

> *Table* **16.1** *General:*

Add BSCR and BSIR to the Glossary.

Item (3p)

The DIM diagram in Figure 1 could usefully show the TVR against the BSn wall, followed closely by an 'Input Selection' box. Likewise in the DOM diagram the TVG against the RBSn wall closely preceded by the '32x32 Crossbar' box. The resulting pleasant symmetry is not completely accidental.

Item (3q)

1PPS waveform in Figure 2 *could show potential falling edges at each BSn transition point (strictly speaking at each falling edge of CLOCK; this diagram happens to show the special case of* f_{CLOCK}*=BSCR)*

Likewise in Figure 4 *the trailing edge of 1PPS should fall on a falling CLOCK edge.*

Item (3r)

"bitstream", "bit stream" *or* "bit-stream"*?*

I believe we have both converged to the hyphenated form, but doubtless there are still instances of the first two forms throughout the text.

4. References

Item (4a)

"VSI Interconnect Hardware Specifications", D.F., proposed 13/3/00.

Item (4b)

"Derivation of the Hardware Specs", D.F., 15/3/00
