Draft VLBI Standard Hardware Interface Specification – VSI-H

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1. Introduction

This document defines a VLBI Hardware Standard Interface (VSI-H) to and from a VLBI 'Data Transmission System' (DTS) that allows heterogeneous DTS's to be interfaced to both data-acquisition system (DAS) and data-processing system (DPS) with a minimum of effort. The interface is defined to be compatible with traditional recording/playback systems, network data transmission and even direct-connect systems. It is designed to completely hide the detailed characteristics of the DTS and allow the data to be transferred from DAS to DPS in a transparent manner.

The VSI-H specification defines the notion of a 'channel quantum', which is the maximum data rate that can be carried on a single standard VSI-H data connector. The basic VSI-H specification specifies a 'channel quantum' of 1.024 Gbps on a single 80-pin connector, with extensions to 2.048 and 4.096 Gbps. Higher data rates may be realized simply by parallel use of two or more 'quantum channels'.

A VLBI Standard *Software* Standard Interface (VSI-S) to accompany VSI-H is proposed but does not yet exist.

2. Intent of the VSI-H Specification

The intent of the VSI-H specification is to define a standard electrical and timing interface, along with a control *philosophy*. In this sense, VSI-H is not intended to be completely 'plug and play', and will require at least some software customization in each case; the future adoption of a VSI-S specification will hopefully minimize the software customization as well. Nevertheless, the adoption of a standardized interface at the hardware level should help to relieve many of the existing incompatibilities that now exist between various VLBI data systems.

The VSI-H specification is primarily aimed at normal data-taking and data-correlation tasks commonplace to VLBI. However, note will also be made of other related activities such as translation of tape media (i.e. tape copying) and parallel operation of multiple DTS's.

3. Structure of the VSI-H Specification

The VSI-H specification is structured as a *base* specification plus a set of *optional extensions*. Adherence to the optional extensions is desirable but not mandatory.

4. Levels of Compliance

Full compliance with the VSI-H specification is expected for all *future* systems designed by parties agreeing to the VSI-H specification. Existing systems are expected to be modified to comply on a *best-effort* basis only. For the purpose of indicating the degree of compliance to the VSI-H standard, two levels of compliance are established:

Level A – Fully compliant with the base VSI-H specification

Level B – Compliant with the VSI-H base spec *except* for one or more of the following:

1. Support for fewer than 32 bit streams
2. Incomplete signal-switching or active-signal-selection capability
3. Incomplete support of all CLOCK frequencies
4. Lack of support for PDATA/QDATA and/or PVALID/QVALID signals
5. Incomplete test-vector capability
6. Data-replacement format

5. Assumptions on which VSI-H Specification is Based

The VSI-H specification is based on the following set of assumptions:

- The DTS is fundamentally a receiver and transmitter of parallel *bit streams* between a Data-Acquisition System and a Data Processing System.
- The *meaning* of individual bit streams is not specified; normally, a bit-stream will be a stream of sign or magnitude bits associated with particular samples, but the actual meaning is to be mutually agreed upon between the DAS and DPS.
- The received and transmitted bit-stream clock rates may be different (e.g. the playback rate into the DPS may be speeded-up or slowed-down), however all bit-stream clock rates on acquisition must be the same, and all bit-stream clock rates on transmit must be the same.
- A single time-tag applies to all parallel bit streams. The DAS time-tag of every bit in every bit-stream must be fully recoverable at the output of the DTS.

6. DTS Structure

For the purposes of the VSI-H specification, the DTS is divided into two logical modules, as indicated in Figure 1:

1. The 'Data Input Module' (DIM) is responsible for accepting multiple parallel bit streams, accompanied by a common clock and common 1-second tick, applying a common time-tag ('observe time'), and sending them to a *transmission media* (tape, disc, fiber-optic, etc.).
2. The 'Data Output Module' (DOM) accepts data from the *transmission media*, decodes the accompanying 'observe-time' information, and recreates the data-streams in accordance with an external clock and '1-second' tick.

The DIM and DOM may reside either in a single physical module or in separate physical modules.

7. Data Input Module (DIM)

A simplified model of one 'quantum channel' of the Data Input Module is shown in Figure 1.

7.1 *DIM Interface*

1. Input signals from the DAS to the DIM–
   a) 32 parallel bit streams, BS_0 thru BS_{31}, all at the same rate, which may be sampled by the DIM at user-selectable rates of 2, 4, 8, 16 or 32 Mbps/bit-stream for a maximum aggregate data rate of 1.024 Gbps for one 'quantum channel'. Optional extension to rates of 64 and 128 Mbps/bit-stream provide maximum aggregate rates of 2.048 and 4.096 Gbps, respectively.
   b) A CLOCK signal accompanying the input bit streams.
   c) A 1PPS tick which defines the corresponding parallel data bits which are to be time-tagged on the integer second. The 1PPS signal is timed to coincide with the data bit taken at the second tick. An ALT1PPS may also be provided from an external asynchronous source, such as a hydrogen maser, to substitute for 1PPS.
   d) A PVALID signal that specifies the 'validity' of the BS_n bit streams. Content and use of the PVALID signal is not defined by the VSI-H specification.

e) A standard 8-bit ASCII asynchronous serial data stream, PDATA, which may send a burst of up to 2048 bytes of information between each 1PPS tick. The content and use of this information is not specified by the VSI-H specification.

2. Control Interface
   The DIM control interface is a 2-way communications interface, implemented in both RS-423 and Ethernet, and normally connected to a computer. The control interface both controls and monitors the operation of the DIM. The DIM controller must be aware of 1PPS ticks to the extent that certain critical messages can be reliably sent to the DIM between specific 1PPS pulses, and that certain messages can be reliably transmitted from the DIM between specific adjacent 1PPS pulses.

7.2 *The Data-Observe-Time (DOT) Clock*

As shown in Figure 1, the DIM maintains an internal Data-Observe-Time (DOT) clock which has the following properties:

1. The DOT clock is the master clock within the DIM, and is used to unambiguously mark each incoming data bit with its current reading to the full resolution of CLOCK.
2. The DOT clock may be set to a specified second of time (presumably UTC) on a given 1PPS or ALT1PPS tick.
3. Once set, the DOT clock keeps time solely by counting CLOCK cycles (i.e. subsequent 1PPS/ALT1PPS ticks are ignored by the DOT clock unless the DOT clock is expressly commanded to be reset).

7.3 *Example of DIM Operation*

The following is an example of a typical sequence of operations of a DIM in a normal observing situation:

1. Through the Control Interface, the DIM is configured to accept any particular subset of 1, 2, 4, 8, 16 or 32 of the incoming bit-streams, all at a specified bit-rate. Only these specified bit streams will be accepted by the DIM and relayed to the *transmission media.*
2. Through the Control Interface, the DOT clock is commanded to be set to a specified integer second of time on the *next* 1PPS (or ALT1PPS) tick [see Note 6 below]. Once set, the DOT clock keeps time by counting cycles of CLOCK, ignoring subsequent 1PPS/ALT1PPS signals. The Dot1pps monitor signal allows confirmation of the DOT epoch setting.
3. Through the Control Interface, the DIM is commanded to begin transmitting the selected input bit streams to the *transmission media.* Each bit in each data stream must be transmitted with its accompanying time tag, either explicitly or implicitly.
4. At the end of the observing period, the DIM is commanded (through the Control Interface) to cease transmitting data.

Notes:

1. The method the DIM uses to record/transmit data or to time-tag data is irrelevant to the VSI-H specification.
2. Each type of DIM may have various control and configuration requirements which are outside the VSI-H specification.
3. It is the responsibility of the DAS to implement any data multiplexing or de-multiplexing that may be necessary to create actual data streams. The DIM only transmits *bit streams*.

4. Some DIM systems may have the ability to transmit additional low-data-rate information, such as bit-stream identification and high-level global validity (i.e. 'antenna on-source'), in addition to the bit-streams themselves. Such information may be transmitted to the DIM via the Control Interface or, in some cases, via the PDATA and/or PVALID data streams.
5. With the exception of ALT1PPS, Dot1pps and the Control Interface, all DIM interface signals are contained in a single 80-pin connector (see Section 12.1).
6. The Control Interface must be designed so that the controlling computer can, on request, be notified in a timely way of the occurrence of a 1PPS/ALT1PPS tick so that the control computer can unambiguously command the DIM to set the DOT clock to a specified integer second of time on the *next* 1PPS/ALT1PPS tick. The subsequent relationship between 1PPS/ALT1PPS and Dot1pps can then be monitored either internally within the DIM [preferred] or externally to verify the 1PPS/ALT1PPS vs Dot1pps relationship. In addition, the control computer should be able to verify the DOT epoch by requesting that the DIM report the DOT setting at the occurrence of the *next* Dot1pps tick.

8. Data Output Module (DOM)

A simplified model of the Data Output Module is shown in Figure 1.

8.1 *DOM Interface*

Input timing signals from the DPS –

1. A clock, DPSCLOCK, from the DPS which acts as a reference frequency for the DOM.
2. A '1-pps tick', DPS1PPS, which is used to set an internal DOM clock called the 'Reconstructed Observe Time' (ROT) clock to an integer-second epoch in a manner similar to the way 1PPS sets the DOT clock in the DIM.

Output signals from the DOM to the DPS –

1. Reconstructed bit streams, RBS_0 thru RBS_{31}, accompanied by a common re-constructed clock (RCLOCK) and 1-pps (R1PPS). With the exception that the RBS_n and R1PPS signals may be speeded up or slowed down relative to the rate at which they entered the DIM, they are identical reproductions of those entering the DIM. The maximum number of reconstructed bit streams corresponds to the number transmitted by the DIM (1, 2, 4, 8, 16 or 32); signal switching within the DOM allows an arbitrary mapping of bit streams to the actual DOM outputs RBS_0 to RBS_{31}.
2. RCLOCK – the clock accompanying the reconstructed bit streams
3. ROT1PPS - 1pps tick from ROT clock
4. R1PPS – reconstructed 1PPS accompanying the bit streams.
5. QVALID – a 1-bit global signal indicating that the reconstructed data are believed to be correct (i.e. tape is reproducing properly). May optionally be extended to include more sophisticated validity indications.
6. QDATA – A standard 8-bit ASCII serial data stream, QDATA, which may send a burst of up to 2048 bytes of information between each 1PPS tick. The content and use of this information is not specified by the VSI-H specification.
7. Control Interface --The DOM control interface is a 2-way communications interface, encompassing *both* RS-423 and Ethernet, which both controls and monitors the operation of the DOM. The DOM controller must be aware of

DPS1PPS to the extent that certain messages can be reliably sent to/from the DOM between specific adjacent DPS1PPS pulses.

8.2 *The Requested Observe Time (ROT) Clock*

The DOM maintains an internal Requested-Observe-Time (ROT) clock which maintains the time to which the re-constructed data are to be synchronized. The ROT clock has the following properties:

1. The ROT clock is set to a specified second of time on a given DPS1PPS tick.
2. Once set, the ROT clock keeps time solely by counting DPSCLOCK cycles (i.e. subsequent DPS1PPS ticks are ignored unless the ROT is expressly commanded to be reset). The monitor signal Rot1pps allows confirmation of the ROT epoch setting.
3. Some DOM's may allow the output data rate to be speeded up by a factor of 2^n. In such a case, the ROT-clock-increment per DPSCLOCK-cycle must be commanded to correspondingly increase. The rate of the R1PPS will correspondingly increase.

8.3 *Delay Offset (extension)*

As indicated in Figure 1, the DOM may include the capability to offset the delay of the reconstructed bit-streams with respect to the ROT clock by a specified arbitrary bit offset, either positive or negative, as specified through the Control Interface. This allows adjustment of the data delay into the DPS for processing. When the delay offset is set to a non-zero value, the RBS_n data streams and R1PPS signals are delayed with respect to the ROT1PPS tick by the amount specified. When the delay offset is zero, ROT1PPS and R1PPS are coincident. QVALID, of course, must also be delayed as necessary to properly align with the data. This capability is most usefully implemented with the capability to precisely track a delay model (a set of spline coefficients, for example) to minimize or eliminate model-based delay adjustments in the DPS[1]. See also notes on PDATA/QDATA usage in Section 15.2.

Note that the delay offset capability can be implemented entirely as a separate module at the output of the DOM.

8.4 *Example of DOM Operation*

The following is an example of a typical sequence of operations of a DOM in a common tape-playback situation:

1. Through the Control Interface, the DOM is configured to reproduce any desired subset of the bit streams sent to it by the DIM.
2. Through the Control interface, the ROT is commanded to be set to a specified UTC integer second of time on the *next* DPS1PPS tick. Once set, the ROT clock keeps time by counting cycles of DPSCLOCK, ignoring subsequent DPS1PPS signals.
3. Through the Control Interface, the DOM is commanded to begin transmitting the selected input bit streams *synchronized to the ROT clock or specified time offset (if delay option if implemented) from the ROT clock.* For tape-playback systems, this means the DOM must use a combination of mechanical tape positioning and electronic buffering to synchronize the recorded data to the ROT clock. When the output data are properly synchronized and valid, the PVALID signal is asserted logical 'true'.

[1] If the reproduced bit streams are multiplexed, some additional fine-delay adjustments may need to be made in the correlator after de-multiplexing.

4. At the end of the data-period of interest, the DOM is commanded (through the Control Interface) to cease transmitting data.

Notes:

1. Note that the reconstructed data streams from the DOM are, except possibly for the data-stream clock rate and for playback errors or intentionally replaced data (see Section 15.1), identical to the data passed from the DAS to the DIM.
2. It is the responsibility of the DPS to do any manipulations necessary to transform the reconstructed bit streams into usable data (such as multiplexing or demultiplexing).
3. Some DOM systems may have the ability to transmit additional low-data-rate information, such as bit-stream identification, etc. in addition to the bit-streams themselves. Such information may be accessed in the DOM via the Control Interface or, in some cases, via the QDATA serial-data stream. When performing a tape-copying operation, QDATA may be used in conjunction with its DIM counterpart, PDATA, to transfer time-tag data to execute simple tape copying operations.
4. Since the DPS is presumed to have some internal buffering, R1PPS/ROT1PPS and RCLOCK need not be precisely aligned with DPS1PPS and DPSCLOCK.
5. With the exception of DPS1PPS, DPSCLOCK, ROT1PPS and the Control Interface, all DOM interface signals are contained in a single 80-pin connector (see Section 12.2).
6. The procedure for setting and monitoring of the ROT clock is similar to that for the DOT clock in the DIM. The notes above concerning these DIM procedures also apply to the DOM.

9. Signal Selection and Switching

9.1 *DIM*

As implied in the discussions above, the DIM must include the capability to select as 'active' *any* subset of 1, 2, 4, 8 or 16 of the 32 potential BS_n input data streams. Only the selected set of bit-streams is required to be transmitted to the DOM. This enables the DTS to more efficiently use the transmission media in cases of reduced aggregrate data rates.

9.2 *DOM*

The DOM is required to reconstruct only the selected set of bit-streams transmitted to it by the DIM. However, the DOM must include the capability to connect *any* of the reconstructed bit-streams to any DOM RBS_n output bit-stream. Figure 1 shows a 32x32 crossbar switch as a functional illustration of this capability, but the designer is free to implement this specification in any satisfactory manner, including a separate external module.

10. Signal Descriptions

10.1 *DIM Input Signals*

Signal	Frequency/Period	Voltage	Comments
CLOCK	See Table 2; Variability up to ±100 ppm	LVDS	CLOCK frequency sets maximum BS_n sample rate; variability to allow for high-velocity spacecraft applications
1PPS	1 per inverse CLOCK frequency (e.g. 1 per $32x10^6$ CLOCK cycles for 32 MHz CLOCK	LVDS	Rising edge should be synchronous with rising edge of data bit to be tagged as 'taken on the second tick' (the 'TOST'

	32 MHz CLOCK		bit); see Figure 2
ALT1PPS	Alternate 1PPS signal	LVDS	May be asynchronous with CLOCK
BS_n n=0 to 31	Allowed sample rates dependent on CLOCK frequency according to Table 2	LVDS	For all clock rates, TOST bit (see Section 11) must be coincident with 1PPS; accept one data bit every 2^k CLOCK cycles thereafter
PDATA	115 kbaud 8-bit serial data	LVDS	Up to 2048 bytes to be received *between* each 1PPS tick

Table 1: DIM Input Signals

CLOCK [RCLOCK] (MHz)	**BS_n sample rate [RBS_n data rate] (Mbps)**						
	2	**4**	**8**	**16**	**32**	**64**	**128**
2	Y						
4	Y	Y					
8	Y	Y	Y				
16	Y	Y	Y	Y			
32	Y	Y	Y	Y	Y		
64 (opt)	Y	Y	Y	Y	Y	Y	
128 (opt)	Y	Y	Y	Y	Y	Y	Y

Table 2: Allowed combinations of clock frequencies and bit-stream data rates

Table 2 notes:

1. 'Y' indicates required
2. 'opt' indicates optional
3. Clock frequencies of 64 and 128 MHz are extensions to the VSI-H standard.

Notes:

1. Use of ALT1PPS is intended for systems where the station 1PPS coming from an independent external source such as a hydrogen maser. In such a case, the ALT1PPS cannot be guaranteed to be synchronous with CLOCK, which may result in a ±1 CLOCK cycle ambiguity in the setting of the DOT clock. This will normally be of little concern so long as the DOT clock is not subsequently reset, which could cause a timing discontinuity.
2. Strictly speaking, the ALT1PPS signal need only be a single pulse to set the DOT clock, but is typically a repetitive signal at a 1-pps rate. Following the setting of the DOT clock, the Dot1pps monitor signal generated by the DOT clock is a useful indicator of proper DOT-clock synchronization.
3. Each input bit-stream, BS_n, is sampled by the DIM only once every CLOCK/2^k periods of CLOCK, where k is set by the operating point in Table 2. This allows, for example, the DAS samplers to always run at CLOCK, even though the data bit-streams are sampled at a lower rate by the DIM.
4. The inclusion of PDATA is primarily for future use, particularly for tape copying, where the output of a DOM can be connected directly to the input of a DIM. In such a case, the QDATA output from the DOM can dynamically transmit data time to the DIM to automatically update the DOT clock. Other uses of PDATA are also possible (see Section 15.2).
5. Any change in the frequency of CLOCK, other than the allowed variability of ±100 ppm, will normally require the DIM, including the DOT clock, to be reset.

10.2 *DIM Output Signals*

Signal	Frequency/Period	Voltage	Comments
Dot1pps	Same as 1PPS	TTL	For monitor purposes only

Table 3: DIM Output Signals

Notes:
1. The Dot1pps signal provides a useful monitor that indicates the DOT is properly synchronized to 1PPS/ALT1PPS.
2. The inclusion in the DIM of other useful monitor signals is also encouraged.

10.3 *DOM Input Signals*

Signal	Frequency/Period	Voltage	Comments
DPSCLOCK	Allowed frequency dependent on frequency of RCLOCK, as shown in Table 5; Variability up to ±100 ppm	LVDS	Sets max output bit-stream rate; variability to allow for high-velocity spacecraft applications
DPS1PPS	1 per inverse CLOCK frequency (e.g. 1 per $32x10^6$ CLOCK cycles for 32 MHz CLOCK	LVDS	Sets epoch of ROT clock second tick

Table 4: DOM Input Signals

Notes:
1. The DPS1PPS signals is used only once to set the ROT clock epoch upon command, presumably at the beginning of a scan or tape.
2. Any change in the frequency of DPSCLOCK, other than the allow variability of ±100 ppm, will normally require the DOM, including the ROT clock, to be reset.

DPSCLOCK (MHz)	RCLOCK (MHz)						
	2	**4**	**8**	**16**	**32**	**64**	**128**
2	Y						
4	Y	Y					
8	Y	Y	Y				
16	Y	Y	Y	Y			
32	Y	Y	Y	Y	Y		
64 (opt)	Y	Y	Y	Y	Y	Y	
128 (opt)	Y	Y	Y	Y	Y	Y	Y

Table 5: Allowed frequency combinations of DPSCLOCK and RCLOCK

Table 5 notes:
1. 'Y' indicates required
2. 'opt' indicates optional
3. CLOCK frequencies of 64 and 128 MHz are extensions to the VSI-H standard.

10.4 *DOM Output Signals*

Signal	Frequency/Period	Voltage	Comments
RCLOCK	Allowed frequencies dependent on DPSCLOCK, according to Table 5	LVDS	Sets max output bit-stream rate
R1PPS	1 pulse per second of ROT clock time	LVDS	May be 1, 2, 4, 8 or 16 R1PPS pulses per DPS1PPS, depending on DOM speedup factor

ROT1PPS	Same as R1PPS	LVDS	Coincident with R1PPS if delay=0 or delay option not implemented
RBS_n n=0 to 31	CLOCK/2^k, k=0,1,2,3,4; (see Notes below)	LVDS	Same as DIM input rate, with possible speedup factor; may be re-mapped (see Notes below)
VALID	Global logical indication that data is sync'ed and valid; no period	LVDS	
QDATA	115 kbaud 8-bit serial data	LVDS	Up to 2048 bytes to be transmitted *between* R1PPS ticks
Rot1pps	Same as ROT1PPS	TTL	For monitor purpose only

Table 6: DOM Output Signals

Notes:
1. Speed-up/slowdown on DOM playback is optional and may not be possible with all systems.
2. If the DOM is operating with a speedup/slowdown, the ROT increment per DPSCLK must be specified to the DOM.
3. The DOM must include the functionality to map any reproduced bit-stream to any of the RBS_n outputs. This is illustrated in Figure 1 as a 32x32 crossbar switch just prior to the output of the DOM, but the desired functionality can be achieved in other ways. Note that the addition of an external 32x32 crossbar switch between the DOM output and the DPS input will also create the required functionality.

10.5 *Validity per bit-stream (proposed extension)*

Some DTS systems may benefit by having the capability to specify per-bit validity at the DOM output for each bit-stream individually. This can be accomplished with no additional hardware by employing a 'bi-phase' code on each of the RBS_n output bit-streams. This works by using the second half of each RBS bit cell to indicate the validity state of that bit, so that the negative-going transition of RCLOCK samples the validity state of each bit cell of every RBS_n; this means that the effective RBS data rate is doubled. Coding is chosen so that a *change* of level in the second half of the bit cell signifies invalidation; this coding means that a bit stream without per-bit-validation is identical to a fully-valid bit stream with per-bit-validition. A DPS may choose to use this information or not. Note that adding this capability has no impact on the base VSI-H specification.

The bi-phase coding scheme is quite common in commercial applications. Note that only *DOM-generated* signals are affected; these validity states are *not* transmitted from the DIM to DOM. The conditions used to control the per-bit-stream validation signals may be specified by the user and are dependent on the details of the DTS system.

11. Signal Timing

11.1 *General*

Figure 2 shows the timing relationships between 1PPS, CLOCK and BS_n; timing relationships between R1PPS, RCLOCK and RBS_n are similar. Two different clock frequencies are shown to illustrate that the epoch of the first sample taken after the rising edge of the 1PPS tick (the so-called 'TOST' sample) must maintain a constant timing relationship with respect to 1PPS regardless of the CLOCK frequency or bit-stream

sample rate. This guarantees that the epoch of the sampled data stream will not change with clock frequency or sample rate. After the TOST sample, subsequent samples are taken every 2^k CLOCK cycles, depending on the ratio of CLOCK frequency to sample rate.

11.2 *Timing Ticks*

Table 7 specifies the minimum and maximum durations of various periodic ticks:

Signal	Type	Min duration	Max duration
1PPS	LVDS	1 cycle of CLOCK	500 ns (inverse 2 MHz)
ALT1PPS	LVDS	1 cycle of CLOCK	No specification
DPS1PPS	LVDS	1 cycle of DPSCLOCK	500 ns
R1PPS	LVDS	1 cycle of RCLOCK	500 ns
ROT1PPS	LVDS	1 cycle of RCLOCK	500 ns
Dot1pps	TTL	Stretched for easy viewing	~10 ms
Rot1pps	TTL	Stretched for easy viewing	~10 ms

Table 7: Timing Tick Min/Max Durations

11.3 *LVDS*

Figure 2 indicates the definitions of the relevant timing parameters for the LVDS signals at the DIM/DOM interfaces. Table 8 specifies the values for these parameters for each of the possible clock rates as seen at the output of a DOM. Table 9 applies to the values as seen at the input to a DIM.

Clock Rate	T_c	T_r max.	T_f max.	T_{ch} min.	T_{ch} max.	T_{cq} min.	T_{cq} max.
32 MHz	31.25	1	1	$0.45T_c$	$0.55T_c$	-1.5	1.5
64 MHz	15.625	1	1	$0.45T_c$	$0.55T_c$	-1.5	1.5
128 MHz	7.8125	1	1	$0.45T_c$	$0.55T_c$	-1.5	1.5

Table 8: Timing Parameters at DOM Output
(All times in Nanoseconds)

Note: Skew (part to part and intrapart) is encompassed in T_{cq}

Clock Rate	T_c	T_r max.	T_f max.	T_{ch} min.	T_{ch} max.	T_{cq} min.	T_{cq} max.
32 MHz	31.25	6	6	$0.4T_c$	$0.5T_c$	6	6
64 MHz	15.625	3	3	$0.4T_c$	$0.5T_c$	2.6	2.6
128 MHz	7.8125	1.6	1.6	$0.4T_c$	$0.5T_c$	1.8	1.8

Table 9: Timing Parameters at DIM Input
(All times in Nanoseconds)

Notes:

1. Cable effects are assumed to cause increase in rise and fall times, as well as in signal skew.
2. Received jitter is assumed to be limited to 5% of the clock period.

11.4 *TTL*

The two monitor signals, Dot1pps and Rot1pps are the only TTL signals defined in the VSI-H specification; both are to be designed to drive into 50-ohms. The rising edge of these signals is the active transition. Duration is to be stretched to be conveniently observed on an oscilloscope. The nominal time offset from 1PPS/ALT1PPS to Dot1pps and from DPS1PPS to Rot1pps should be provided to the user and is, ideally, independent of CLOCK/DSPCLOCK frequencies.

12. Connectors/Pinouts/Cables

12.1 *DIM*

80-pin female MDR connector with the following LVDS signals (pinout in Table 10):

PVALID
PDATA
CLOCK
1PPS
BS_0-BS_{31}

14-pin MDR connector with the following LVDS signals (pinout in Table 11):

ALT1PPS
(Note: If DIM and DOM are in the same physical box, this same connector will also carry DPSCLOCK and DPS1PPS)

Dot1pps: TTL on 50Ω BNC connector

Control Interface (may be shared with DOM if in same physical box):

RS-423: RJ-45 (pinout in Table 12)
Ethernet: RJ-45 jack (10Base-T or 10/100 Base-T)

12.2 *DOM*

80-pin female MDR connector with the following LVDS signals (pinout in Table10):

ROT1PPS
QVALID
QDATA
RCLOCK
R1PPS
RBS_0-RBS_{31}

14-pin MDR connector with the following LVDS signals (pinout in Table 11):

DPSCLOCK
DPS1PPS
(Note: If DIM and DOM are in the same physical box, this same connector will also carry ALT1PPS)

Rot1pps: TTL on 50Ω BNC connector

Control Interface (may be shared with DIM if in same physical box):

RS-423: RJ-45 (pinout in Table 12)
Ethernet: RJ-45 jack (10Base-T or 10/100 Base-T)

DIM	DOM	Pin(+)	Pin(-)
-	ROT1PPS	1	41
PVALID	QVALID	2	42
PDATA	QDATA	3	43
CLOCK	RCLOCK	4	44
1PPS	R1PPS	5	45
BS_0	RBS_0	6	46
BS_j	RBS_j	j+6	j+46

BS31	RBS31	37	77
Unused	Unused	38-40	78-80

Table 10: MDR-80 Pinouts

Signal	Pin(+)	Pin(-)
ALT1PPS	1	8
DPS1PPS	2	9
DPSCLOCK	3	10
Unused	4-7	11-14

Table 11: MDR-14 Pinout

Signal	Pin	Comments
RTS (out)	1	not used by DTS
DTR (out)	2	not used by DTS
TX+ (out)	3	
TX- (gnd)	4	
RX- (gnd)	5	
RX+ (in)	6	
DSR (in)	7	not used by DTS
CTS (in)	8	not used by DTS

Table 12: RJ-45 (RS-423) Pinout[2]

12.3 *Unused LVDS Connector Pins*

All pins on LVDS connectors designated as 'unused' must have an active transmitter and receiver attached; transmitter will be held at static '0' or '1'.

12.4 *LVDS Grounding*

No LVDS-connector pins are assigned to ground. Ground is normally carried through on the cable-assembly shield.

12.5 *LVDS Cabling*

Signals are allowed to flow only in one direction on a single LVDS cable.

Maximum LVDS cable length is a function of clock rate. According to specifications (see References), clock rates of 32 MHz, 64 MHz and 128 MHz can be supported at maximum cable lengths of approximately 100m, 60m and 40m, respectively. For purposes of the VSI-H specification, the maximum cable length is set by the LVDS signal timing specifications in Section 11.4; in practice, a cable length of at least 20m should be readily achievable.

12.6 *LVDS Device Standards*

All LVDS devices used in the DTS must meet the TIA/EIA-644 standard.

[2] 'In' and 'Out' designations are from DTS point of view. Pin assignments are such that either a 'straight-thru' or 'crossover' RJ-45 cable can be used depending on whether host port is DTE or DCE.

13. Control Interfaces

The DIM and the DOM shall have *both* an Ethernet *and* an RS-423 control interface. Both may be simultaneously active, though not required. Some of the control and monitor functions, as discussed above, are quasi-real-time, in that control/monitor data must be reliably communicated between 1PPS pulses (in the DIM) or DPS1PPS pulses (in the DOM) in order to properly set and monitor the DOT and ROT clocks.

If the DIM and DOM are in the same physical box, they may share the Ethernet and RS-423 control interfaces.

The details of the communications messages and protocols are to be specified in the VSI-S document.

The specifications of the control interfaces are:

1. RS-423: operating at least to 9600 baud, preferably higher (to 115 kbaud); 8-bit, 1 stop bit, no parity; Xon/Xoff handshaking
2. Ethernet: 10Base-T or 10/100Base-T

14. Test Vectors

Test-vector generators (TVG) and receivers (TVR) are used to validate the physical layer connections between the Data Acquisition System (DAS), Data Input Module (DIM), Data Output Module (DOM), and Data Processing System (DPS) components of the VLBI Data Transfer System (DTS).

The VSI-H specification imposes no requirements on testing the interface through the transmission media from the DIM to the DOM, though designers are urged to implement testing procedures suitable to the characteristics of the DTS.

14.1 *General Characteristics*

The philosophy of the TV specification is to fully test the connection of user equipment to the DIM and DOM data interfaces. To this end, the TV system should have the following characteristics (see Figure 1):

1. The DIM must include a TVR to validate data transmission from equipment connected to the DIM data interface.
2. The DOM must include a TVG to validate data transmission from the DOM to external equipment.
3. Each TVG is capable of generating 32 unique pseudo-random noise (PRN) bit streams, denoted as TV_0-TV_{31}, each of a fixed period of 2^{15}-1 (32767) bits.
4. All PRN bit-streams are re-synchronized at each 1PPS/R1PPS epoch.
5. The TV bit-stream data rate is always at the rate of the data which it replaces. This implies that TV rates must be consistent with Table 2.

Though the VSI-H specification does not directly extend to the DAS or DTS, a complete TV system would also include a TVG in the DAS[3] and a TVR in the DTS.

14.2 *Test Vector Generator*

Figure 3 shows an example gate-level design of the TVG (based on Crestech design) to be used in VSI-H compliant DTS's. Each of the 32 output PNS bit-streams is re-

[3] Including a TVG in the DAS probably only makes sense when the DIM receives and uses 1PPS from the DAS. The use of an asynchronous ALT1PPS makes the use of a DAS-TVG difficult.

initialized at each 1PPS/R1PPS tick. Table 13 tabulates the first 20-bits of each of the 32 TV bit-streams. Each bit stream has an approximate balance of the number of 'ones' and 'zeroes', corresponding to a 'DC-bias' of ~50%. Note that, for illustration purposes, the CLOCK signal in Figure 3 is shown to have the same frequency as the data-bit-stream sample rate.

In addition, each TVG must be capable of producing an "all 0's" or "all 1's" signal on all 32 bit-stream outputs. In this mode, it is useful to verify that the TVR's reports an error rate of ~50%.

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}	t_{16}	t_{17}	t_{18}	t_{19}	t_{20}
TV_0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
TV_1	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0	0
TV_2	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	0	0	0
TV_3	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0
TV_4	0	0	0	0	0	1	1	1	0	1	1	0	1	1	1	0	0	0	0	1
TV_5	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	0	0	0	0	1
TV_6	0	0	0	0	1	0	1	1	1	0	0	1	0	1	1	0	0	0	1	1
TV_7	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
TV_8	0	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	1	1	1
TV_9	0	0	0	1	0	1	0	0	0	0	1	0	1	0	1	0	0	1	1	1
TV_{10}	0	0	1	1	1	0	0	0	0	1	1	1	0	1	1	0	1	0	0	1
TV_{11}	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0
TV_{12}	0	1	1	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	0	0
TV_{13}	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
TV_{14}	1	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0
TV_{15}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
TV_{16}	1	1	1	1	1	1	1	0	1	1	1	0	1	0	1	1	1	1	1	1
TV_{17}	1	1	1	1	1	1	1	0	1	1	1	0	1	0	0	1	1	1	1	1
TV_{18}	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1	1
TV_{19}	1	1	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	1
TV_{20}	1	1	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1	1	0
TV_{21}	1	1	1	1	1	0	1	0	1	0	1	1	0	1	0	1	1	1	1	0
TV_{22}	1	1	1	1	0	1	0	0	0	1	1	0	1	0	0	1	1	1	0	0
TV_{23}	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
TV_{24}	1	1	1	0	1	0	0	1	1	1	0	1	0	0	0	1	1	0	0	0
TV_{25}	1	1	1	0	1	0	1	1	1	1	0	1	0	1	0	1	1	0	0	0
TV_{26}	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	1	1	0
TV_{27}	1	1	1	0	1	1	1	1	1	1	0	1	1	1	0	1	1	0	0	1
TV_{28}	1	0	0	1	1	1	1	1	0	0	1	1	0	0	0	0	1	0	1	1
TV_{29}	1	0	1	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1
TV_{30}	0	1	1	1	1	1	1	0	1	1	1	0	1	0	1	0	1	1	1	1
TV_{31}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1

Table 13: TVG data outputs for first 20 data bits following 1PPS/R1PPS

14.3 *Test Vector Timing Relationships*

As indicated in Figure 4, the TVG is initialized at every 1PPS/R1PPS tick in such a way that the 'TOST bit' at t_0 is undefined. From that point forward, the TVG increments every sample clock period and has the same timing relationship to CLOCK as normal user data. The TVG continuously cycles through the 32767-bit TVG sequence until the next 1PPS/R1PPS tick, at which point the TVG is again re-initialized.

14.4 *Test Vector Receiver*

On command, the DIM-TVR will measure and report the bit-error rate (BER) and "DC-bias" on each of the 32 input test bit-streams, either sequentially or simultaneously. In order to untangle possible bit-stream 'mix-ups' (i.e. bit streams being directed to the wrong place), the TVR must be able to examine each possible bit stream for each of the 32 possible TV sequences.

TVR reporting periods are to be flexible, but are restricted to correspond to an integer number of 1PPS/R1PPS periods.

15. Other Notes and Comments:

15.1 *Data-Replacement Format*

Some systems may periodically replace small portions of data sampled by the DIM with timing and synchronization information. The use of a 'data-replacement' format under the VSI-H standard is allowed but not encouraged, and such systems would be granted only Level B compliance status. The QVALID signal must accurately flag any replacement data as 'invalid' as it emerges from the DOM. In addition, the use of standard VSI-H test-vector testing with the DAS and DPS may be difficult or impossible with a data-replacement format.

15.2 *Usage of PDATA/QDATA*

The use of the PDATA/QDATA asynchronous serial-ASCII signals is not specified under the VSI-H specification. A few possible uses of these signals are:

Media translation: During media-translation (i.e. tape copying) operations, where the DOM output is connected to the DIM input, QDATA may be used to transmit the high-level time (e.g. date and time to the unit-second level) to the PDATA input of the DIM between each R1PPS tick. In this case, it is probably most useful if the QDATA time tag corresponds to the epoch of the *next* R1PPS tick. This allows the DIM to dynamically set the DOT clock to the proper time at the next 1PPS (R1PPS) tick in much the same way the DOT clock is set in normal operation. Other auxiliary information may, of course, be transmitted between the DIM and DOM in the same way.

Auxiliary information from DAS: If the DAS is capable of supplying PDATA information to the DIM, this information may be used as the DIM sees fit. Possible information might include time, data-collection parameters, antenna pointing, system temperature, etc. If the system is capable, some or all of this information may be used to control the DIM, or perhaps transmitted to the DOM for output to QDATA.

Model parameters to DPS: An attractive possible use of QDATA is to periodically transmit station-model information to the DPS, which can in turn use it to process the data. This capability is particularly attractive if the DOM includes the capability to delay the data according to a dynamic model supplied to it by the host computer. If, for

example, the ROT clocks of all DOM's are set to represent a center-of-earth clock and each DOM dynamically delays it output data according to a center-of-earth model, the DOM output data may be immediately available for correlation processing with only a small amount of FIFO re-synchronizing (using ROT1PPS tick) necessary in the DPS. The QDATA model parameters, transmitted between each ROT1PPS tick, would need only to carry such information as fractional bit delay, rate, plus a phase model for each channel, in order to provide the DPS with all necessary information to do proper processing.

15.3 *Usage of PVALID/QVALID*

The VSI-H specifies the use of the QVALID signal only to the extent that it indicates the global validity status of the DOM output data streams. If available to the DIM, the PVALID signal may be used to indicate that the DAS output data are 'valid'. This information can be used by the DIM as it sees fit, including transmitting it to the DOM for inclusion as a factor in controlling it QVALID output. If the DOM is sufficiently capable, the QVALID signal may also be used, for example, as a pulsar-gating mechanism to the DPS; the pulsar gating capability may be further augmented by specifying gating on an individual bit-stream basis to account for the frequency-dispersive nature of pulsar timing (see Section 10.5).

15.4 *Media Translation (Tape Copying)*

With the use of the VSI-H interfaces, data may be easily copied from one media to another in a straightforward manner. The output of a DOM may be directly connected to the DIM input. For this purpose, the DOM must have the capability of 'standalone playback' without the connection of DPSCLK or DPS1PPS signals. In such case, the ROT clock will be commanded to simply track the playback time on the tape.

Time-tag transfer between DOM and DIM can be accomplished by two different methods. By using the DOM facility to transmit the ROT setting immediately following a R1PPS tick, a control computer can read the ROT and appropriately set the DOT clock in the DIM. Once ROT and DOT clocks are appropriately set, copying will take place with no further intervention until a time discontinuity (tape stop and restart, for example) when the DOT and ROT clocks must again be reset. Alternatively, time-tag transfer from DOM to DIM can be done through the QDATA/PDATA serial data lines (as discussed above).

15.5 *Multiple Parallel DTS's*

In the event that a single DTS is not able to handle the required aggregate data rate, multiple DTS's may be employed in parallel. In the case of the DIM, the DAS must be able to support multiple DIM's in parallel, each being supported as if it were standalone. Multiple parallel DOM's can be handled in the same way.

15.6 *Multi-Port DTS*

A DTS may support multiple quantum channels simply by the inclusion of multiple MDR-80 data connectors on the DIM and DOM. Only a single MDR-14 connector for other timing signals is required. VSI-H imposes no requirements on signal connectivity between quantum channels within a multi-port DTS.

16. Glossary

16.1 *General*

BER	Bit Error Rate
DAS	Data Acquisition System; provides parallel bit-stream data to DIM
DIM	Data Input Module
DOM	Data Output Module
DOT	Data Observe Time; maintained in DIM
DPS	Data Processing System (most often a correlator)
DTS	Data Transmission System; includes DIM and DOM
LVDS	Low-Voltage Differential Signaling
'Quantum Channel'	The data carried on a single VSI 80-pin connector; all VSI-compliant DTS's must support an aggregrate data rate of 1.024 Gbps, plus a specified set of lower data rates.
ROT	Requested Observe Time; maintained in DOM
Sample Rate	The rate at which incoming bit-streams to the DIM are sampled by the DIM.
TOST bit	Data bit 'Taken On the Second Tick'; the TOST bit maintains a constant relationship to 1PPS and is always transmitted regardless of the bit-stream sample rate.
TV	Test Vector
TVG	Test Vector Generator
TVR	Test Vector Receiver
UTC	Universal Coordinated Time
VSI	VLBI Standard Interface
VSI-H	VSI Hardware Specification
VSI-S	VSI Software Specification

16.2 *Signals*

Name	Function	Format	Description
1PPS	DIM input	LVDS	One-second tick
ALT1PPS	DIM input	TTL	Alternate one-second tick
BS_n	DIM input	LVDS	Bit-stream n
CLOCK	DIM input	LVDS	Data clock
Dot1pps	DIM output	TTL	DOT clock 1-pps epoch monitor
DPS1PPS	DOM input	LVDS	DPS one-second tick to DOM
DPSCLOCK	DOM input	LVDS	DPS clock to DOM
PDATA	DIM input	LVDS	115 kbaud asynchronous 8-bit data; up to 2048 bytes per 1PPS 'tick'; content unspecified by VSI-H
PVALID	DIM input	LVDS	Global 'data-valid'
QDATA	DOM output	LVDS	115 kbaud asynchronous 8-bit data; up to 2048 bytes per 1PPS 'tick'; content unspecified by VSI-H

QVALID	DOM output	LVDS	Global ‘data valid’
R1PPS	DOM output	LVDS	‘Reconstructed’ 1PPS
RBSn	DOM output	LVDS	‘Reconstructed’ bit-stream n
RCLOCK	DOM output	LVDS	‘Reconstructed’ data clock
ROT1PPS	DOM output	LVDS	ROT clock 1-pps
Rot1pps	DOM output	TTL	ROT clock monitor

17. References

3M Connectors:

http://www.mmm.com/Interconnects/prod_con_0531.html

3M Pleated Foil Cable Assemblies:

http://www.mmm.com/Interconnects/Prod_cas_0804.html

TI LVDS Devices:

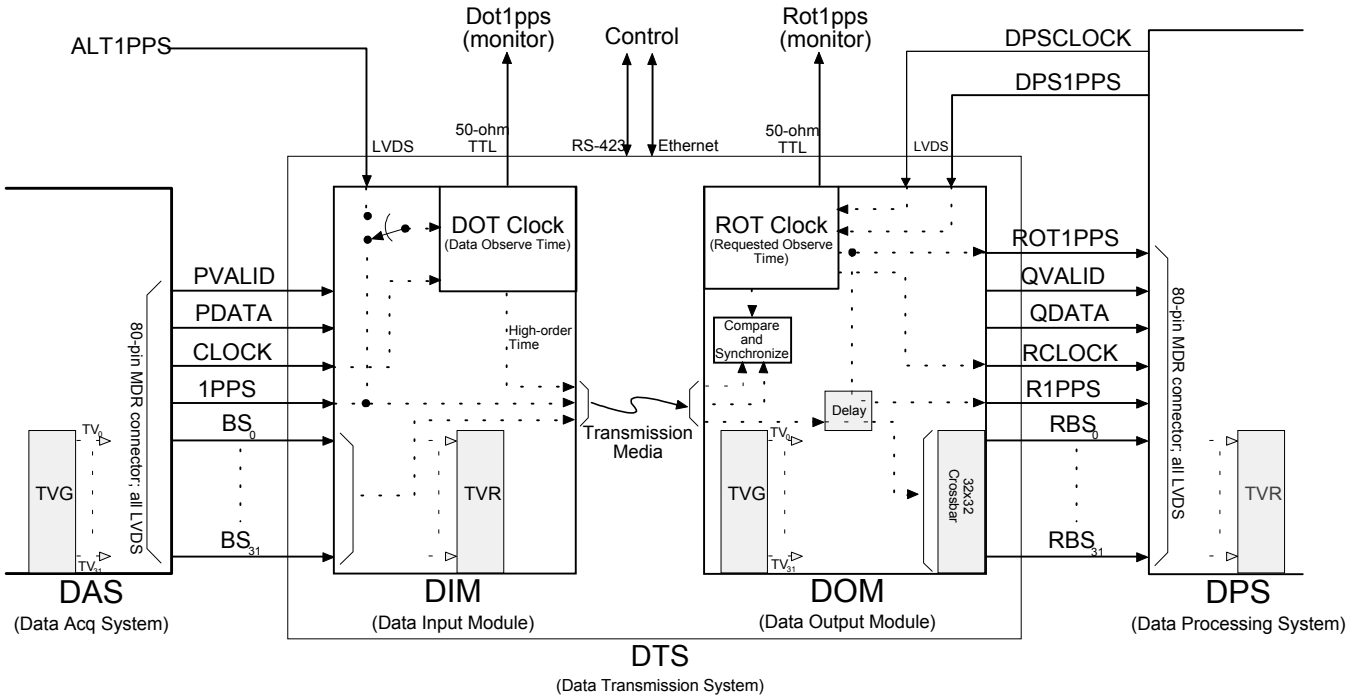
http://www.ti.com/sc/docs/schome.html

(At this site, perform “SC Parameter Search” for ‘LVDS’)

National Semiconductor Application Notes:

http://www.national.com/apnotes/

(At this site, you can find the application notes by number or by category.)



Notes:
1. Shaded items are for illustrative purposes only.
2. PVALID is optionally transmitted from DIM to DOM.
3. PDATA is optionally transmitted from DIM to DOM.
4. Data delay in DOM is optional.
5. If DIM/DOM in single box, ALT1PPS/DPSCLOCK/DPS1PPS share single MDR-14 connector.
6. This diagram does not show all functions and options -- see VSI-H specification for details.

Figure 1: VSI-H Functional Block Diagram

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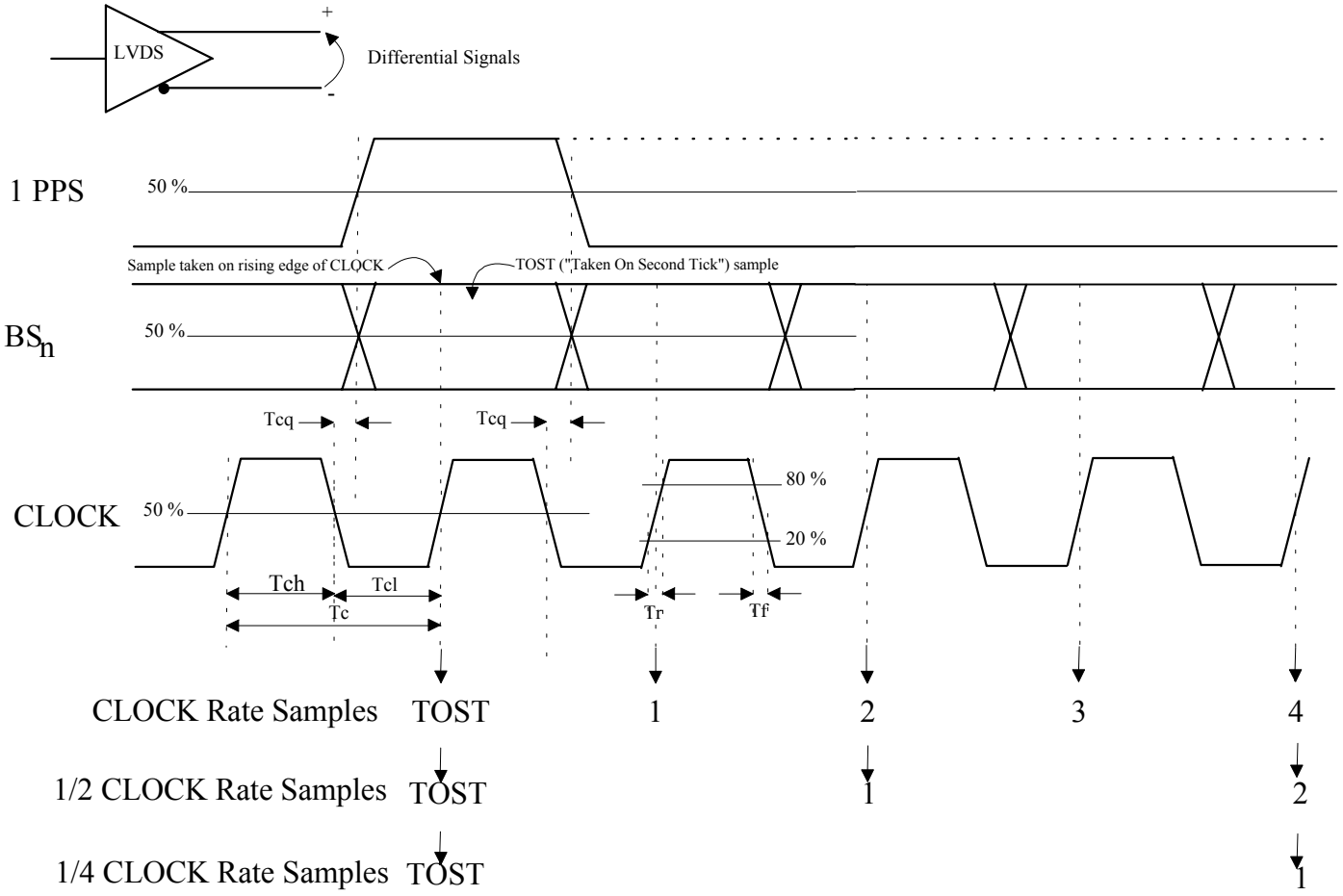
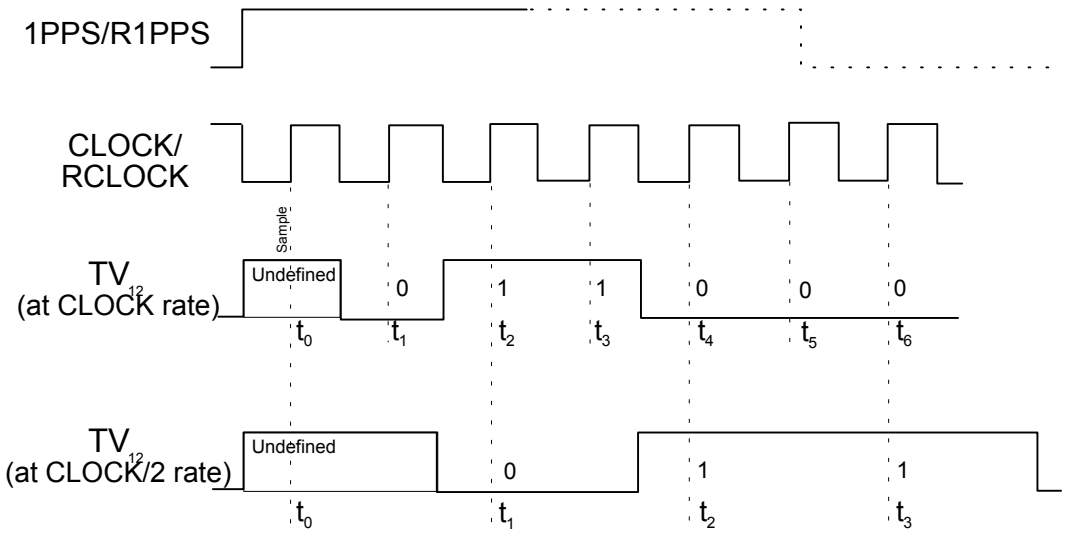


Figure 2: LVDS Timing Parameters

VSI_TIM2.DRW



Notes:

1. TV_{12} bit stream is shown for illustration.
2. The TV data streams have exactly the same timing relationship to CLOCK/RCLOCK and 1PPS/R1PPS as actual data streams.
3. The TVG is initialized on every 1PPS/R1PPS tick. The TV value at t0 is undefined.
4. Starting with t1, the TVG continuously cycles through the 32767-bit TVG sequence until the next 1PPS/R1PPS tick, at which point the TVG is again re-initialized.

Figure 4: TVG Timing Relationships

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