Updated Draft Proposal for
VLBI Standard Interface (VSI-H) Specification

29 January 2000

Table of Contents

1. Introduction

This document defines a VLBI Hardware Standard Interface (VSI-H) to and from a VLBI 'Data Transmission System' (DTS) that allows heterogeneous DTS's to be interfaced to both data-acquisition system (DAS) and data-processing system (DPS) with a minimum of effort. The interface is defined to be compatible with traditional recording/playback systems, network data transmission and even direct-connect systems. It is designed to completely hide the detailed characteristics of the DTS and allow the data to be transferred from DAS to DPS in a transparent manner.

A VLBI Standard *Software* Standard Interface (VSI-S) to accompany VSI-H is proposed but does not yet exist.

2. Intent of the VSI-H Specification

The intent of the VSI-H specification is to define a standard electrical and timing interface, along with a control *philosophy*. In this sense, VSI-H is not intended to be completely 'plug and play', and will require at least some software customization in each case; the future adoption of a VSI-S specification will hopefully minimize the software customization as well. Nevertheless, the adoption of a standardized interface at the hardware level should help to relieve many of the existing incompatibilities that now exist between various VLBI data systems.

The VSI-H specification is primarily aimed at normal data-taking and data-correlation tasks commonplace to VLBI. However, note will also be made to other related activities such as translation of tape media (i.e. tape copying) and parallel operation of multiple DTS's.

3. Structure of the VSI-H Specification

The VSI-H specification is structured as a *base* specification plus a set of *optional extensions*. All VSI-H compliant systems must adhere at least to the base specification. Adherence to the optional extensions is desirable but not mandatory.

4. Assumptions on which VSI-H Specification is Based

The VSI-H specification is based on the following set of assumptions:

- The DTS is fundamentally a receiver and transmitter of parallel *bit streams* between a Data-Acquisition System and a Data Processing System.
- The *meaning* of individual bit streams is not specified; normally, a bit-stream will be a stream of sign or magnitude bits associated with particular samples, but the actual meaning is to be mutually agreed upon between the DAS and DPS.
- The received and transmitted bit-stream clock rates may be different (e.g. the playback rate into the DPS may be speeded-up or slowed-down), however all bit-stream clock rates on acquisition must be the same, and all bit-stream clock rates on transmit must be the same.
- A single time-tag applies to all parallel bit streams. The DAS time-tag of every bit in every bit-stream must be fully recoverable at the output of the DTS.

5. Discussion

For the purposes of the VSI-H specification, the DTS is divided into two logical modules, as indicated in Figure 1:

1. The 'Data Input Module' (DIM) is responsible for accepting multiple parallel bit streams, accompanied by a common clock and common 1-second tick, applying a common time-tag ('observe time'), and sending them to a *transmission media* (tape, disc, fiber-optic, etc.).
2. The 'Data Output Module' (DOM) accepts data from the *transmission media*, decodes the accompanying 'observe-time' information, and recreates the data-streams in accordance with an external clock and '1-second' tick.

The DIM and DOM may reside either in a single physical module or in separate physical modules.

6. Data Input Module (DIM)

A simplified model of the basic Data Input Module is shown in Figure 1.

6.1 *DIM Interface*

1. Input signals from the DAS to the DIM–
   a) 32 parallel bit streams, BS_0 thru BS_{31}, all at the same bit rate, which may be chosen to be 2, 4, 8, 16 or 32 Mbps/bit-stream.
   b) A CLOCK signal at a constant rate of 32 MHz.
   c) A 1PPS tick which defines the corresponding parallel data bits to be time-tagged on the integer second. The 1PPS signal is timed to coincide with the data bit taken at the second tick. An ALT1PPS may also be provided from an external asynchronous source, such as a hydrogen maser, to substitute for 1PPS.
   d) An (optional) standard 8-bit ASCII serial data stream, PDATA, which may send a burst of up to 2048 bytes of information between each 1PPS tick. The content of this information is not specified by VSI-H.
   a) Control Interface
      The DIM control interface is a 2-way communications interface, implemented in both RS-232 and Ethernet, and normally connected to a computer. The control interface both controls and monitors the operation of the DIM. The DIM controller must be aware of 1PPS ticks to the extent that certain critical messages can be reliably sent to the DIM between specific 1PPS pulses, and that certain messages can be reliably transmitted from the DIM between specific adjacent 1PPS pulses.

6.2 *The Data-Observe-Time (DOT) Clock*

As shown in Figure 1, the DIM maintains an internal Data-Observe-Time (DOT) clock which has the following properties:

1. The DOT clock is the master clock within the DIM, and is used to unambiguously mark every each incoming data bit with its current reading to the full resolution of CLOCK.
2. The DOT clock may be set to a specified second of time (presumably UTC) on a given 1PPS or ALT1PPS tick.

3. Once set, the DOT clock keeps time solely by counting CLOCK cycles (i.e. subsequent 1PPS/ALT1PPS ticks are ignored unless the DOT is expressly commanded to be reset).

6.3 *Example of DIM Operation*

The following is an example of a typical sequence of operations of a DIM in a normal observing situation:

1. Through the Control Interface, the DIM is configured to accept any particular set of 2, 4, 8, 16 or 32 of the incoming bit-streams, all at a specified bit-rate. Only these specified bit streams will be accepted by the DIM and relayed to the *transmission media.*
2. Through the Control Interface, the DOT clock is commanded to be set to a specified integer second of time on the *next* 1PPS (or ALT1PPS) tick [see Note 6 below]. Once set, the DOT clock keeps time by counting cycles of CLOCK, ignoring subsequent 1PPS/ALT1PPS signals. The monitor signal DOT1PPS allows confirmation of the DOT epoch setting.
3. Through the Control Interface, the DIM is commanded to begin transmitting the selected input bit streams to the *transmission media.* Each bit in each data stream must be transmitted with its accompanying time tag, either explicit or implicit.
4. At the end of the observing period, the DIM is commanded (through the Control Interface) to cease transmitting data.

Notes:

1. The method the DIM uses to record/transmit data or to time-tag data is irrelevant to the VSI-H specification.
2. Each type of DIM may have various control and configuration requirements which are outside the VSI-H specification.
3. It is the responsibility of the DAS to implement any data multiplexing or de-multiplexing that may be necessary to create actual data streams. The DIM only transmits *bit streams*.
4. Some DIM systems may have the ability to transmit additional low-data-rate information, such as bit-stream identification and high-level global validity (i.e. 'antenna on-source'), in addition to the bit-streams themselves. Such information may be transmitted to the DIM via the Control Interface or, in some cases, via the PDATA serial-data stream. When performing a tape-copying operation, for example, PDATA may be used in conjunction with its DOM counterpart, QDATA, to transfer time data necessary to occasionally reset the DOT clock (see Notes and Comments in Section 13).
5. With the exception of ALT1PPS, DOT1PPS and the Control Interface, all DIM interface signals are contained in a single 80-pin connector (see Section 10).
6. The Control Interface must be designed so that the controlling computer can, on request, be notified in a timely way of the occurrence of a 1PPS/ALT1PPS tick so that the control computer can unambiguously command the DIM to set the DOT clock to a specified integer second of time on the *next* 1PPS/ALT1PPS tick. The subsequent relationship between 1PPS/ALT1PPS and DOT1PPS can then be monitored either internally within the DIM [preferred] or externally to verify the 1PPS/ALT1PPS vs

DOT1PPS relationship. In addition, the control computer should be able to verify the DOT epoch by requesting that the DIM report the DOT setting at the occurrence of the *next* DOT1PPS tick.

7. Data Output Module (DOM)

A simplified model of the Data Output Module is shown in Figure 1.

7.1 *DOM Interface*

1. Output signals from the DOM to the DPS –
   a. Reconstructed bit streams, RBS_0 thru RBS_{31}, accompanied by a common reconstructed CLOCK (RCLOCK) and reconstructed 1PPS (R1PPS). With the exception that these signals may be speeded up or slowed down relative to the rate which they entered the DIM, they are identical reproductions of those entering the DIM.[1] The maximum number of reconstructed bit streams corresponds to the number transmitted by the DIM (2, 4, 8, 16 or 32), though crossbar switching within the DOM allows an arbitrary mapping of bit streams to the actual DOM outputs RBS_0 to RBS_{31}.
   b. VALID – a 1-bit global signal indicating that the reconstructed data are believed to be correct (i.e. tape is reproducing properly).
   c. (Optional) Each reconstructed bit stream (RBS_n) is accompanied by a 'data valid' signal (V_n) which indicates whether the data are believed to be valid or invalid on a bit-by-bit basis. The V_n signals, if present, are carried on a separate connector.
2. Input timing signals from the DPS –
   a. A clock, DPSCLOCK, from the DPS which acts as a reference frequency from which RCLOCK is derived. This clock is at a constant 32 MHz frequency regardless of the bit rate of the reconstructed bit streams.
   b. A '1-pps tick', DPS1PPS, which is used to set an internal DOM clock called the 'ROT clock' to a integer-second epoch in a manner similar to the way 1PPS sets the DOT clock in the DIM.
   c. Control Interface --The DOM control interface is a 2-way communications interface, RS-232 and Ethernet, normally connected to a computer, which both controls and monitors the operation of the DOM. The DOM controller must be aware of DPS1PPS to the extent that certain messages can be reliably sent to/from the DOM between specific adjacent DPS1PPS (or ALTDPS1PPS) pulses.
   d. The signals ALTDPSCLK and ALTDPS1PPS, contained in a separate connector, may be used in place of DPSCLOCK and DPS1PPS, respectively, as indicated in Figure 1.

[1] Some DIM's (such as Mark III/IV recording systems) periodically replace small portions of the data with synchronization and time code information. In these cases, the DOM must flag such 'replacement data' as invalid.

7.2 *The Requested Observe Time (ROT) Clock*

The DOM maintains an internal Requested-Observe-Time (ROT) clock which maintains the time to which the re-constructed data are to be synchronized. The ROT clock has the following properties:

a. The ROT clock is set to a specified second of time on a given DPS1PPS tick.
b. Once set, the ROT clock keeps time solely by counting DPSCLOCK cycles (i.e. subsequent DPS1PPS ticks are ignored unless the ROT is expressly commanded to be reset). The monitor signal ROT1PPS allows confirmation of the ROT epoch setting.
c. Some DOM's may allow the output data rate to be speeded up by a factor of 2^n. In such a case, the ROT-clock-increment per DPSCLOCK-cycle must be commanded to correspondingly increase by the same factor. The DPSCLOCK frequency will not change.

7.3 *Example of DOM Operation*

The following is an example of a typical sequence of operations of a DOM in a common tape-playback situation:

1. Through the Control Interface, the DOM is configured to reproduce any desired subset of the bit streams sent to it by the DIM.
2. Through the Control interface, the ROT is commanded to be set to a specified UTC integer second of time on the *next* DPS1PPS tick. Once set, the ROT clock keeps time by counting cycles of DPSCLOCK, ignoring subsequent DPS1PPS signals.
3. Through the Control Interface, the DOM is commanded to begin transmitting the selected input bit streams *synchronized to the ROT clock.* For tape-playback systems, this means the DOM must use a combination of mechanical tape positioning and electronic buffering to synchronize the recorded data to the ROT clock. When the output data are properly synchronized and valid, the VALID signal is asserted logical 'true'.
4. At the end of the data-period of interest, the DOM is commanded (through the Control Interface) to cease transmitting data.

Notes:

1. Note that the reconstructed data streams from the DOM are, except possibly for the data-stream clock rate and for playback errors or intentionally replaced data, identical to the data passed from the DAS to the DIM.
2. It is the responsibility of the DPS to do any manipulations necessary to transform the reconstructed bit streams into usable data (such as multiplexing or demultiplexing).
3. Some DOM systems may have the ability to transmit additional low-data-rate information, such as bit-stream identification, etc. in addition to the bit-streams themselves. Such information may be accessed in the DOM via the Control Interface or, in some cases, via the QDATA serial-data stream. When performing a tape-copying operation, QDATA may be used in conjunction with its DIM counterpart, PDATA, to transfer time-tag data to execute simple tape copying operations.
4. Since the DPS is presumed to have some internal buffering, R1PPS and RCLOCK need not be precisely aligned with DPS1PPS and DPSCLOCK.

5. With the exception of ALTDPS1PPS, ALTDPSCLK, ROT1PPS and the Control Interface, all DOM interface signals are contained in a single 80-pin connector (see Section 10). The optional validity signals V_0 thru V_{31}, if present, are contained in an identical parallel 80-pin connector.
6. The procedures for setting and monitoring of the ROT clock is similar to that for the DOT clock in the DIM. The notes above concerning these DIM procedures also apply to the DOM.

8. Signal Descriptions

8.1 *DIM Input Signals*

Signal	Frequency/Period	Voltage	Comments
CLOCK	32 MHz (base); 64/128 MHz (extension); Variability up to ±100 ppm	LVDS	Set max input bit-stream rate; variability to allow for high-velocity spacecraft applications
1PPS	1 per inverse CLOCK frequency (e.g. 1 per $32x10^6$ CLOCK cycles for 32 MHz CLOCK	LVDS	Rising edge should be synchronous with rising edge of data bit to be tagged as 'taken on the second tick' (the 'TOST' bit)
ALT1PPS	Alternate 1PPS signal	TTL	May be asynchronous with CLOCK
BS_n n=0 to 31	CLOCK/2^k, k=0,1,2,3,4; (see Notes below)	LVDS	For all values of k, TOST bit must be coincident with 1PPS; accept a data bit every k^{th} CLOCK cycle thereafter
PDATA	115 kbaud 8-bit serial data	LVDS	Up to 2048 bytes to be received *between* every 1PPS tick

Notes:

1. Use of ALT1PPS is intended for systems where the station 1PPS coming from an independent external source such as a hydrogen maser. In such a case, the ALT1PPS cannot be guaranteed to be synchronous with CLOCK, which may result in a ±1 CLOCK cycle ambiguity in the setting of the DOT clock. This will normally be of little concern so long as the DOT clock is not subsequently reset, which could cause a timing discontinuity.
2. Strictly speaking, 1PPS/ALT1PPS need only be a single pulse to set the DOT clock, but typically they are repetitive signals at the specified rate. Following the setting of the DOT clock, these signals may be useful to monitor the continued synchronization of 1PPS/ALT1PPS with the DOT clock (see DOT1PPS below).
3. Each input bit-stream, BS_n, is sampled by the DIM only once every CLOCK/2^k periods of CLOCK. This allows, for example, the DAS samplers to always run at CLOCK, even for narrow BBC bandwidths.
4. The inclusion of PDATA is primarily for future use, particularly for tape copying, where the output of a DOM can be connected directly to the input of a DIM. In such a case, the QDATA output from the DOM can dynamically transmit data time to the DIM to automatically update the DOT clock. Other uses of PDATA are also possible.

8.2 *DIM Output Signals*

Signal	Frequency/Period	Voltage	Comments
DOT1PPS	Same as 1PPS	TTL(?)	For monitor purposes only

Notes:
1. The DOT1PPS signal provides a useful monitor that the indicates the DOT is properly synchronized to 1PPS/ALT1PPS.
2. The inclusion in the DIM of other useful monitor signals is also encouraged.

8.3 *DOM Input Signals*

Signal	Frequency/Period	Voltage	Comments
DPSCLOCK	32 MHz (base); 64/128 MHz (extension); Variability up to ±100 ppm	LVDS	Sets max output bit-stream rate; variability to allow for high-velocity spacecraft applications
DPS1PPS	1 per inverse CLOCK frequency (e.g. 1 per $32x10^6$ CLOCK cycles for 32 MHz CLOCK	LVDS	Sets epoch of ROT clock second tick
ALTDPSCLK	Alternate to DPSCLOCK	LVDS	On separate connector from DPSCLOCK
ALTDPS1PPS	Alternate to DPS1PPS	LVDS	On separate connector from DPS1PPS

Notes:
1. The DPS1PPS/ALTDPS1PPS signals are used only to set the ROT clock epoch upon command, presumably once per scan or tape, or as the case may be.

8.4 *DOM Output Signals*

Signal	Frequency/Period	Voltage	Comments
RCLOCK	Same as DPSCLOCK	LVDS	Sets max output bit-stream rate
R1PPS	1 pulse per second of ROT clock time	LVDS	May be 1, 2, 4, 8 or 16 R1PPS pulses per DPS1PPS, depending on DOM speedup factor
RBS_n n=0 to 31	$CLOCK/2^k$, k=0,1,2,3,4; (see notes below)	LVDS	Same as DIM input rate, with possible speedup factor; may be re-mapped (see Notes below)
VALID	Global logical indication that data is sync'ed and valid; no period	LVDS	
QDATA	115 kbaud 8-bit serial data	LVDS	Up to 2048 bytes to be transmitted *between* R1PPS ticks
ROT1PPS	Reproduction of R1PPS	TTL(?)	For monitor purposes only

Notes:
1. Only the set of bit-streams selected for input to the DIM can be reproduced by the DOM (obvious).

2. Speed-up on DOM playback is optional and may not be possible with all systems.
3. If the DOM is operating with a speedup (or possibly slowdown?), the ROT increment per DPSCLK must be specified to the DOM.
4. Note that RCLOCK is always at the same frequency as DPSCLOCK. For bit-stream playback rates slower than RCLOCK, the DPS must accept data bits only every 2^k RCLOCK cycles. In that case, care must be taken to properly sample the 'TOST' bit.
5. As indicated in Figure 1, the DOM must include a 32x32 crossbar switch just prior to the output of the RBS_n signals. This allows arbitrary mapping of the reproduced bit streams to the RBS_n outputs for the convenience of the DPS.

8.5 *DOM Output Signals (extension)*

An optional set of validity/bit-stream signals may be included in the DOM output. These signal are carried on a separate, but identical, connector to the normal DOM signals.

Signal	**Frequency/Period**	**Voltage**	**Comments**
VCLOCK	Same as RCLOCK	LVDS	Same as RCLOCK
V1PPS	Same as R1PPS	LVDS	Same as R1PPS
V_n n=0 to 31	Bit-by-bit validity corresponding to RBS_n	LVDS	Logical .TRUE. on good data bit.

Notes:
1. The VCLOCK and V1PPS signals are included to guarantee proper relative timing with the V_n signals. Though the RCLOCK and R1PPS signals may be sufficient for clocking of the V_n signals at 32 MHz, conservative design demands clocking signals within the same connector for potential clock rates of 64 and 128 MHz.

9. Signal Timing

9.1 *LVDS*

Figure 2 indicates the definitions of the relevant timing parameters for the LVDS signals. The following table specifies the quantitative values for these parameters for each of the possible clock rates:

Clock Rate	T_c	T_r Max.	T_f Max.	T_{cu} Min.	T_{cu} Max.	T_{cl} Min.	T_{cl} Max.	T_{cq} Min.	T_{cq} Max.
32 MHz	31.25	4	4	$0.45T_c$	$0.55T_c$	$0.45T_c$	$0.55T_c$	-6	6
64 MHz	15.625	2	2	$0.45T_c$	$0.55T_c$	$0.45T_c$	$0.55T_c$	-3	3
128 MHz	7.8125	1	1	$0.45T_c$	$0.55T_c$	$0.45T_c$	$0.55T_c$	-1.5	1.5

Table 1: LVDS Timing Parameters
(All times in Nanoseconds)

Notes:
1. Skew (part to part and intrapart) is encompassed in T_{cq}.
2. Jitter must be contained in a tolerance on T_c.

3. If opposite edge receive clocking is used, minimum set up time is given by (T_c Min.) - (T_{cq} Max.) – (Cable skew). Similarly, minimum hold time is given by (T_{cu} Min.)+(T_{cq} Min.) – (Cable skew).

9.2 *TTL*

To be done.

10. Connectors/Pinouts

10.1 *DIM*

80-pin female MDR connector containing the following LVDS signals (pinout in Table 2):

PDATA
1PPS
CLOCK
BS_0-BS_{31}

ALT1PPS: TTL on 50Ω BNC (SMA?) connector

DOT1PPS: TTL on 50Ω BNC (SMA?) connector

RS-232: Standard female DB-9 connector wired as DCE (RJ-45?).

Ethernet: RJ-45 (10/100Base-T) [preferred]or BNC (10Base-2)

10.2 *DOM*

80-pin female MDR connector containing the following LVDS signals (pinout in Table 2):

DPS1PPS
DPSCLOCK
VALID
QDATA
R1PPS
RCLOCK
RBS_0-RBS_{31}

Optional extension: 80-pin female MDR connector containing the following LVDS signals (pinout in Table 2):

V1PPS
VCLOCK
V_0-V_{31}

14-pin MDR connector with the following LVDS signals and pinout:

ALTDPSCLK	Pins 3(+) and 10(-)
ALTDPS1PPS	Pins 5(+) and 12(-)

ROT1PPS: TTL on 50Ω BNC (SMA?) connector

RS-232: Standard female DB-9 connector wired as DCE (RJ-45?).

Ethernet: RJ-45 [preferred] or BNC

DIM	DOM	DOM (extension)	Pin(+)	Pin(-)
Unused	Unused	Unused	1	41
-	DPS1PPS	-	2	42
-	DPSCLOCK	-	3	43
-	VALID	-	4	44
PDATA	QDATA	-	5	45
1PPS	R1PPS	V1PPS	6	46
CLOCK	RCLOCK	VCLOCK	7	47
BS_0	RBS_0	V_0	8	48
BS_j	RBS_j	V_j	j+8	j+48
BS31	RBS31	V31	39	79
Unused	Unused	Unused	40	80

Table 2: MDR-80 Pinouts

10.3 *Cable Length*

Maximum cable length of any cable between DAS, DIM, DOM and DPS is 15 meters.

11. Control Interfaces

Both the DIM and the DOM shall have *both* an Ethernet *and* an RS-232 control interface. Both may be simultaneously active, though not required. Some of the control and monitor functions, as discussed above, are quasi-real-time, in that control/monitor data must be reliably communicated between 1PPS pulses (in the DIM) or DPS1PPS pulses (in the DOM) in order to properly set and monitor the DOT and ROT clocks.

The details of the communications messages and protocols is to be specified in the VSI-S document.

Specifications:

RS-232: operating at least to 9600 baud, preferably higher (to 115 kbaud); 8-bit, 1 stop bit, no parity

Ethernet: 10Base-T or 10/100Base-T [preferred]; 10Base-2 (coax) acceptable

12. Test Vectors (extension)

The use of test vector generators (TVG) and receivers (TVR) are strongly recommended to validate the physical layer connections between the Data Acquisition System (DAS), Data Input Module (DIM), Data Output Module (DOM), and Data Processing System (DPS) components of the VLBI Data Transfer System (DTS).

12.1 *General Characteristics*

The philosophy of the TV specification is to fully test each and every signal path through the DTS. To this end, the TV system should have the following characteristics (see Figure 1):

1. The DIM must include both a TVR and a TVG. The TVR must be able to validate TV data from a DAS, a DOM, or from the DIM-TVG. When activated, the TVG replaces the data normally arriving in bit-streams BS_0-BS_{31}.
2. The DOM must include both a TVR and a TVG. The TVR must be able to validate TV data from a DIM of from the DOM-TVG. When activated, the TVG replaces the reconstructed images of bit streams BS_0-BS_{31} at the input to the 32x32 crossbar switch.
3. Each TVG is capable of generating 32 unique pseudo-random noise (PRN) bit streams, denoted as TV_0-TV_{31}, each of a fixed period of 2^{15}-1 (32767) bits.
4. All PRN bit-streams are re-synchronized at each 1PPS/R1PPS epoch.
5. All TV sequences operate at the selected *bit-stream data rate;* that is, the PRN will increment at the selected bit-stream data rate, which is <=CLOCK/RCLOCK.

This set of characteristics provides a powerful capability to test the DTS from end-to-end, as well as in smaller pieces.

Though the VSI-H specification does not directly extend to the DAS or DTS, a complete TV system would also include a TVG in the DAS[2] and a TVR in the DTS.

12.2 *Test Vector Generator*

Figure 3 shows the gate-level design of the TVG to be used in VSI-compliant DTS's. Each of the 32 output PNS bit-streams is re-initialized (re-synchronized) at each 1PPS/R1PPS tick. Table 1 tabulates the first 20-bits of each of the 32 TV bit-streams. Each bit stream has an approximate balance of the number of 'ones' and 'zeroes', corresponding to a 'DC-bias' of ~50%.

The bit rate of the TVG shall be selectable to correspond to the input data rate of 2, 4, 8, 16 or 32 Mbps (with optional extensions to 64 and 128 Mbps).

In addition, each TVG should be capable of producing an "all 0's" or "all 1's" signal on all 32 bit-stream outputs. In this mode, it is useful to verify that the TVR's report an error rate of ~50%.

12.3 *Test Vector Receiver*

The TVR supports the same set of bit-stream data rates as the DIM and DOM. On command, the TVR will measure and report the bit-error rate (BER) and "DC-bias" on each of the 32 input test bit-streams, either sequentially or simultaneously. To do so, the TVR must obviously be told which of the 32 possible PRN sequences it is to expect in

[2] Including a TVG in the DAS probably only makes sense when the DIM receives and uses 1PPS from the DAS. The use of an asynchronous ALT1PPS makes the use of a DAS-TVG difficult.

each bit stream. In order to untangle possible bit-stream 'mix-ups' (i.e. bit streams being directed to the wrong place), the TVR must be able to examine each possible bit stream for each possible PRN.

Normally, the TVR will initiate the correlation of the test bit-stream at the 1PPS/R1PPS second tick. It is also possible to design more sophisticated TVR's which attempt to correlate with a test bit-stream of *any* epoch; such TVR's could prove useful in some circumstances, but are not mandated (this may not be possible; need to discuss – ARW).

TVR reporting periods are to be flexible, but are restricted to correspond to an integer number of 1PPS/R1PPS periods.

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}	t_{16}	t_{17}	t_{18}	t_{19}	t_{20}
TV_0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
TV_1	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0	0
TV_2	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	0	0	0
TV_3	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0
TV_4	0	0	0	0	0	1	1	1	0	1	1	0	1	1	1	0	0	0	0	1
TV_5	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	0	0	0	0	1
TV_6	0	0	0	0	1	0	1	1	1	0	0	1	0	1	1	0	0	0	1	1
TV_7	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
TV_8	0	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	1	1	1
TV_9	0	0	0	1	0	1	0	0	0	0	1	0	1	0	1	0	0	1	1	1
TV_{10}	0	0	1	1	1	0	0	0	0	1	1	1	0	1	1	0	1	0	0	1
TV_{11}	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0
TV_{12}	0	1	1	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	0	0
TV_{13}	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
TV_{14}	1	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0
TV_{15}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
TV_{16}	1	1	1	1	1	1	1	0	1	1	1	0	1	0	1	1	1	1	1	1
TV_{17}	1	1	1	1	1	1	1	0	1	1	1	0	1	0	0	1	1	1	1	1
TV_{18}	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1	1
TV_{19}	1	1	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	1
TV_{20}	1	1	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1	1	0
TV_{21}	1	1	1	1	1	0	1	0	1	0	1	1	0	1	0	1	1	1	1	0
TV_{22}	1	1	1	1	0	1	0	0	0	1	1	0	1	0	0	1	1	1	0	0
TV_{23}	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
TV_{24}	1	1	1	0	1	0	0	1	1	1	0	1	0	0	0	1	1	0	0	0
TV_{25}	1	1	1	0	1	0	1	1	1	1	0	1	0	1	0	1	1	0	0	0
TV_{26}	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	1	1	0
TV_{27}	1	1	1	0	1	1	1	1	1	1	0	1	1	1	0	1	1	0	0	1
TV_{28}	1	0	0	1	1	1	1	1	0	0	1	1	0	0	0	0	1	0	1	1
TV_{29}	1	0	1	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1
TV_{30}	0	1	1	1	1	1	1	0	1	1	1	0	1	0	1	0	1	1	1	1
TV_{31}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
TV_{32}	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0	1	0	1

Table 3: TVG bit-stream outputs for first 20 data bits following 1PPS/R1PPS

12.4 *Test Vector Notes*

Notes:

1. The TVG and TVR are clocked at the selected bit-stream data rate, CLOCK/2^k, not by CLOCK.
2. As currently specified, the TVG is initialized at the occurrence of 1PPS/R1PPS (defined as 't=0' in Figure 3), but the PRN bit sequence does not actually start until 't=1'. Are there consequences of this that need to be discussed?

13. Other Notes and Comments:

13.1 *Media Translation (Tape Copying)*

With the use of the VSI-H interfaces, data may be easily copied from one media to another in a straightforward manner. The output of a DOM may be directly connected to the DIM input. Data connectors are directly compatible. For this purpose, the DOM must have the capability of 'standalone playback' without the connection of DPSCLK or DPS1PPS signals. In such case, the ROT clock will be commanded to simply track the playback time on the tape.

Time-tag transfer between DOM and DIM can be accomplished by two different methods. By using the DOM facility to transmit the ROT setting immediately following a R1PPS tick, a simple control computer can read the ROT and appropriately set the DOT clock in the DIM. Once ROT and DOT clocks are appropriately set, copying will take place with no further intervention. Alternatively, time-tag transfer from DOM to DIM can be done through the QDATA/PDATA serial data lines ('hardware time code') or through the DIM/DOM control interfaces.

13.2 *Multiple Parallel DIM/DOM's*

In the event that a single DTS is not able to handle the required aggregate data rate, multiple DTS's may be employed in parallel. In the case of the DIM, the DAS must be able to support multiple DIM's in parallel, each being supported as if it were standalone. Multiple parallel DOM's are to be handled in the same way.

14. Glossary

14.1 *General*

BER	Bit Error Rate
DAS	Data Acquisition System
DIM	Data Input Module
DOM	Data Output Module
DOT	Data Observe Time
DPS	Data Processing System
DTS	Data Transmission System
LVDS	Low-Voltage Differential Signaling
ROT	Requested Observe Time

TOST bit	Data bit ‘Taken On the Second Tick’; the TOST bit is always transmitted regardless of the declared bit-stream rate.
TVG	Test Vector Generator
TVR	Test Vector Receiver
UTC	Universal Coordinated Time
VSI	VLBI Standard Interface
VSI-H	VSI Hardware Specification
VSI-S	VSI Software Specification
VSI-C	VSI-Channel Specification

14.2 *Signals*

Name	Function	Format	Description
1PPS	DIM input	LVDS	One-second tick
ALT1PPS	DIM input	TTL	Alternate one-second tick
ALTDPS1PPS	DOM input	LVDS	Alternate DPS1PPS
ALTDPSCLK	DOM input	LVDS	Alternate DPSCLK
BS_n	DIM input	LVDS	Bit-stream n
CLOCK	DIM input	LVDS	Data clock
DOT1PPS	DIM output	TTL	DOT clock 1-pps epoch monitor
DPS1PPS	DOM input	LVDS	DPS one-second tick to DOM
DPSCLK	DOM input	LVDS	DPS clock to DOM
PDATA	DIM input	LVDS	115 kbaud asynchronous 8-bit data; up to 2048 bytes per 1PPS ‘tick’; content unspecified by VSI-H
QDATA	DOM output	LVDS	115 kbaud asynchronous 8-bit data; up to 2048 bytes per 1PPS ‘tick’; content unspecified by VSI-H
R1PPS	DOM output	LVDS	‘Reconstructed’ 1PPS
RBSn	DOM output	LVDS	‘Reconstructed’ bit-stream n
RCLOCK	DOM output	LVDS	‘Reconstructed’ data clock
ROT1PPS	DOM output	TTL	ROT clock ‘1-pps’ epoch monitor
RVALID	DOM output	LVDS	‘Reconstructed’ validity
VALID	DIM input	LVDS	Global ‘data valid’

15. References

3M Connectors:
http://www.mmm.com/Interconnects/prod_con_0531.html
3M Pleated Foil Cable Assemblies:
http://www.mmm.com/Interconnects/Prod_cas_0804.html
TI LVDS Devices:
http://www.ti.com/sc/docs/schome.html
(At this site, perform “SC Parameter Search” for ‘LVDS’)
National Semiconductor Application Notes:
http://www.national.com/apnotes/
(At this site, you can find the application notes by number or by category.)

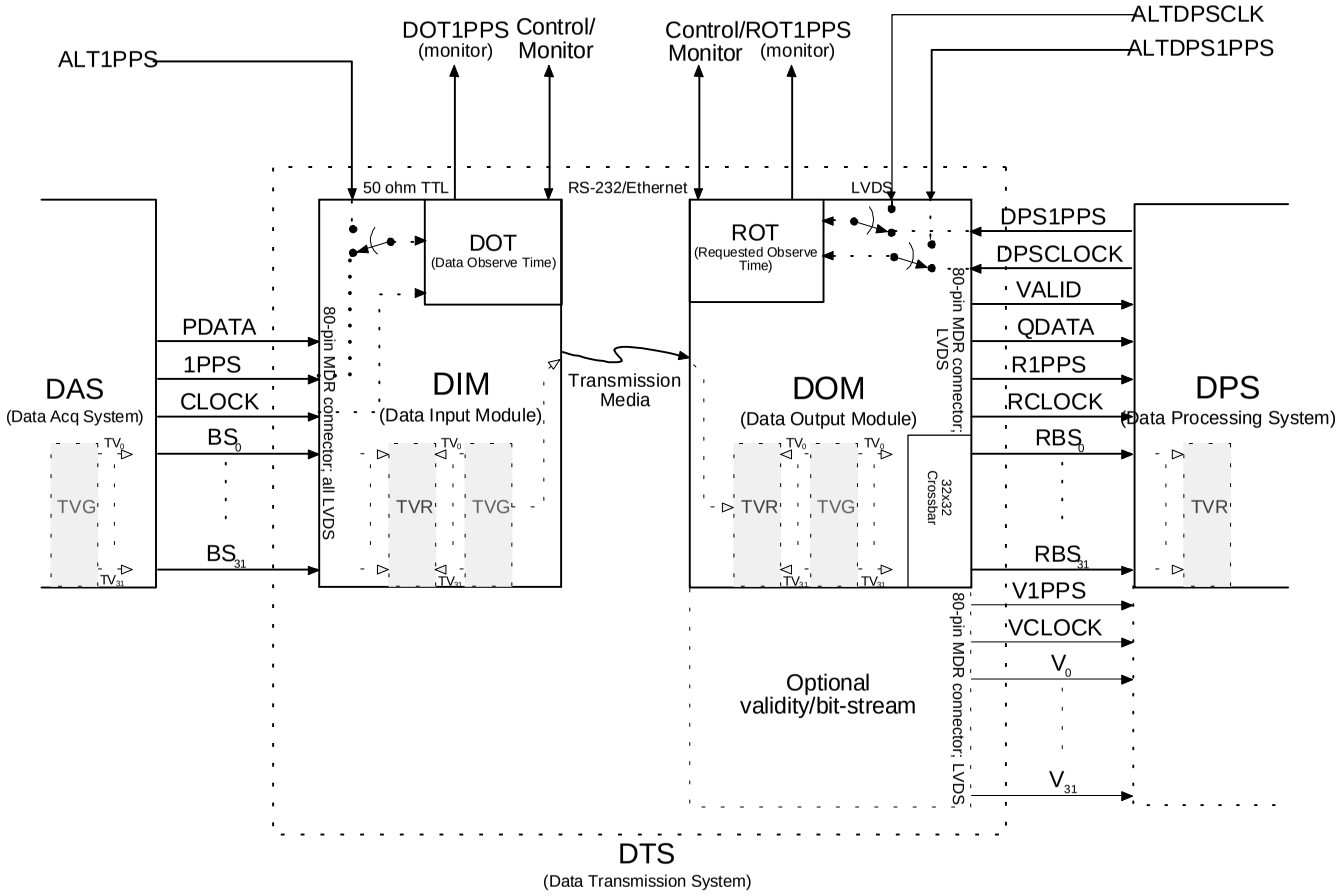

Figure 1: VSI-H Block Diagram

VSI5.DRW
ARW 28 Jan 2000

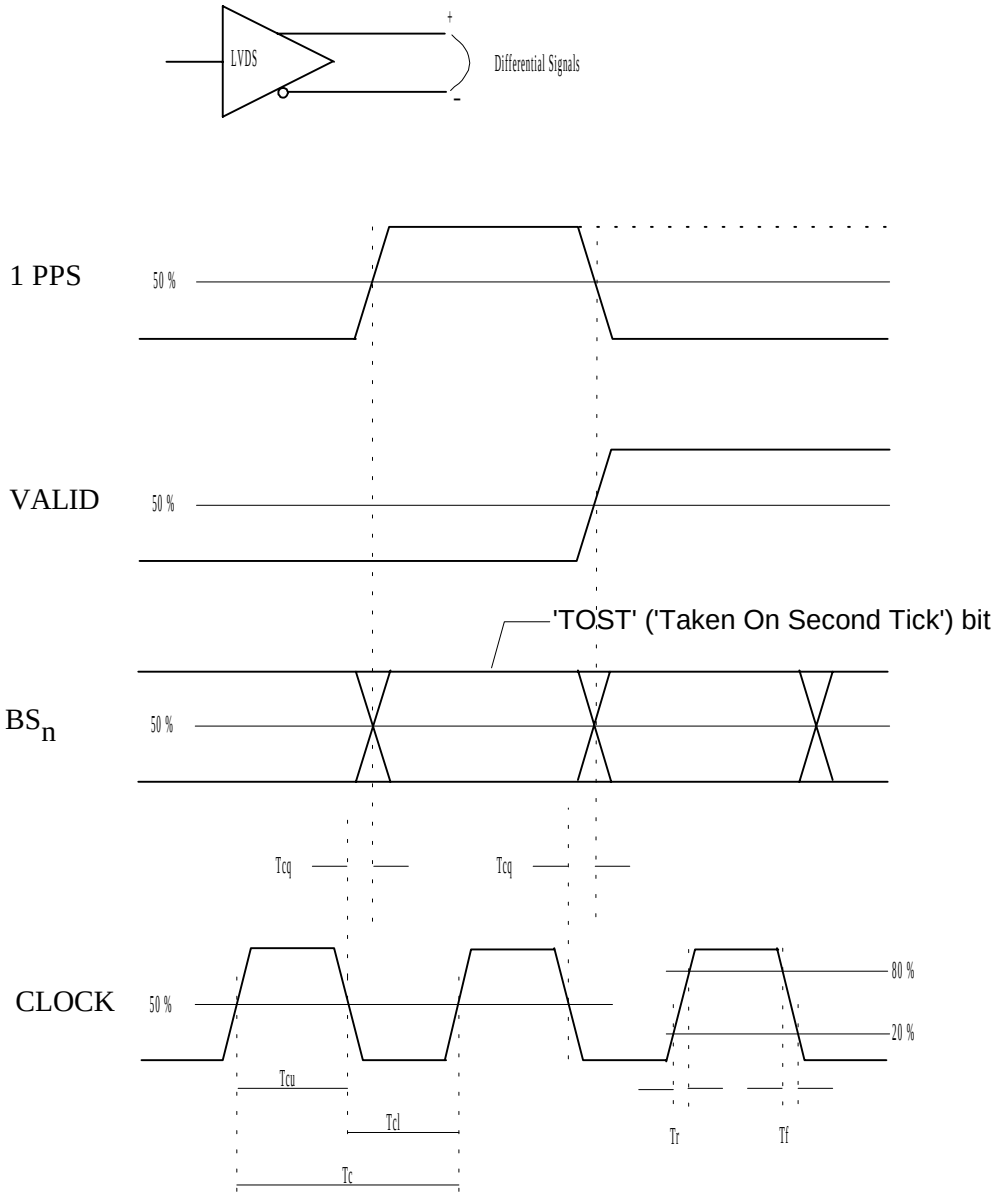

Figure 2: LVDS Timing Parameters

VSI_TIME.DRW
28 Jan 00