Recommendations on Remaining VSI Issues

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Over the past few weeks there has been considerable discussion of various issues regarding VSI. In this note I want try to summarize the current state of affairs of these issues and put forward a proposal in each area which I judge to be as close to consensus as possible. Hopefully we can then have some final discussions and fine tuning of these issues and reach agreement. I will then revise the VSI draft specification document accordingly and distribute it for final approval. I hope that this procedure is satisfactory for everyone. [I had hoped to add full referencing for each item, but simply don't have time if this is to be distributed in time for the 5 Nov Japanese meeting; I will try to add more referencing later.]

For each item there may be listed three categories of specification:

'Proposal' – this would be required
'Recommendation' – recommended, but optional
'Optional' – a useful addition, but definitely optional

Constant Clock Frequency

Proposal: Operation of the DIM and DOM shall be possible with a constant clock frequency (CLOCK or DPSCLOCK) of 64 MHz, regardless of actual bit-stream data rate.

Optional addition: Operation with a constant frequency clock of 32 MHz.

Comment: There seems to be strong support for constant clock frequency operation, and I agree that it should be included in the specification.

References:

Variable-Frequency DOM Clock Rates

Proposal: The DOM shall accept a CORRCLOCK with at least a deviation of +/-1000 ppm from the nominal.

Optional: Much wider range of allowed variation.

Comment: The worst-case clock deviation due to spacecraft motion is on the order of +/-100 ppm, so the +/-1000 ppm spec gives some additional latitude. A much wider range of allowed variation is potentially useful for tape playback systems.

References:

DIM Active Bit Streams

Proposal: Any 1, 2, 4, 8 or 16 DIM input streams on a given DTS port may be designated as 'active'.

Comment: A majority seems to agree to include this as part of the specification; in systems that always transmit 16 bits streams, such as described by Kawaguchi, this might require an internal redistribution of 'active' streams to create 16 streams, but this should neither be too difficult or wasteful of DTS bandwidth since the number of active input streams is 2**n. If this is too difficult as a requirement, it might be demoted to a 'recommendation'.

References:

Bit Stream Remapping

Proposal: An arbitrary mapping may be specified between DIM input-stream numbers and the internal DIM stream numbers (i.e. as is a crossbar switch exists in front of the DIM).

Recommendation: An arbitrary mapping may be specified between the DOM internal bit streams (identical by definition to the DIM internal stream numbers) and the DOM output streams.

Comments: Dick makes a compelling case for re-mapping in the DIM.

Reference: Ferris, 29 Oct 99 'More Comments on VSI'

Test Vectors

Proposal:

1. In the DIM, each bit-stream may be replaced by an internally generated pseudo-noise sequence (PNS) of fixed length 2**15-1 (32767) bits. The PNS will increment at the bit-stream data rate (not necessarily the same as CLOCK). The PNS sequence will be unique for each of the 16 DIM bit streams and be individually controllable (on/off) for each DIM bit stream (for ID purposes). The PNS sequence will be re-initialized at each 1PPS tick. The DIM PNS's will be re-mapped according to the user specification (see above).
2. In the DOM, each output bit stream may be replaced by an internally generated PNS stream with characteristics identical to the PNS streams generated by the DIM. Each DOM PNS stream must be individually controllable
3. The DIM must be able to measure to validate the PNS on each input bit stream (in anticipation that DAS's may eventually be able to provide PNS's, and useful in copying operations)
4. The DOM must be able to validate the PNS on each output bit stream.
5. The set of PNS's will be identical for all DTS's in the world.

Recommendations:

1. The DIM and DOM will measure actual TV error rates.
2. Each TVG may be commanded to all 0's or 1's for test purposes.
3. The DAS should be designed to generate the same set of PNS's.
4. The DPS should be able to validate and measure error rates of the PNS's.

Comment: The coefficients for each of the required 16 PNS's has not yet been specified. By allowing individual control of bit-stream TVG's, as pointed out by Cannon et al, the complications of additional signaling ID can be avoided.

References:
Wietfeldt, 22 Oct 99, 'VSI-H PN Sequence Specification – strawman'
Ferris, 28 Oct 99, 'More Comments on VSI'

Carlson, 28 Oct 99, 'Comments on Dick Ferris' comments'

Hardware Time Code

Proposal:

1. The DOM will output an 'information-signal' using standard asynchronous ASCII codes. This signal will be present in the same connector as the corresponding DOM output bit streams and be user-programmable according to requirements. This signal could be used, for

example, to transmit the time-code (to 1-second resolution) immediately following each R1PPS tick to aid in tape copying. It could also be programmed to, for example, transmit ID information, low-resolution data-validity information, or station model information to the DPS, etc.

2. The DIM will be capable of receiving and decoding this periodically-transmitted signal, though operation of the DIM is not dependent on it.
3. The information signal will be transmitted and received at 115 kbaud.

Comments: I prefer to call this signal some like Programmable Data (PDATA?) or something like that since it potentially has a number of uses.

References:

1PPS Waveform Timing

Proposal: The 1PPS waveform should be one CLOCK-period wide and its transitions must coincide with bit-stream-data transitions. Data coincident with 1PPS are considered to be the data sample taken at the instant of the station second tick. The relationship between the RCLOCK and R1PPS signals follows the same rule. The relationship between DPSCLOCK and DPS1PPS signals also follows the same rule (though there are no actual accompanying data-streams for DPSCLOCK).

Comment: For purposes of the VSI specification, each bit-stream is considered to be a non-multiplexed sample stream, and hence each stream has a well-defined data bit 'taken on the second tick'. In reality, the data streams may already be multiplexed going into the DIM, but neither the DIM nor DOM are aware of this.

References:

ALT1PPS

Proposal: The ALT1PPS signal shall be the rising edge of TTL waveform into a 50-ohm BNC. This signal can be used in place of 1PPS to set the internal DIM clock. ALT1PPS may asynchronous with respect to CLOCK, with the understanding that the particular

Option: An R1PPS monitor signal, dubbed R1PPSMON, may be made available at the DOM as a TTL waveform from a 50-ohm BNC.

References:

Signal Grouping

Proposal:

1. All DIM signals except the ALT1PPS and the normal control signals (Ethernet, RS-232) will be carried on a single multi-pin connector.
2. All DOM signals except the R1PPSMON and the normal control signals (Ethernet, RS-232) will be carried on a single multi-pin connector with pin assignments corresponding to the DIM connector.

Comments:
The signal count is each data cable is now as follows:

16 – bit streams
CLOCK/RCLOCK
1PPS/R1PPS

DPSCLOCK
DPS1PPS
VALID (global)
PDATA

Electrical

Proposal: All signals carried on the data connectors of the DIM and DOM will be differential LVDS.

Comment: LVDS will easily carry the 64 MHz signals. LVDS is quite common these days and several sources of LVDS electronics are available.

Connector and Cable Specifications

Proposal: MDR/3M 50-pin connector (see Dick Ferris, 30 July 99, p. 21)

Comments: The number of signals (22) mandates the use of the 50-pin MDR connector if all signals are DLVDS. At Haystack have been doing some investigation of this connector and the cables the corresponding cables. The MDR connector has the advantages of small size, mass termination and mechanical lockdown. With the proper cable, we believe (but have not yet empirically confirmed) that 15m cable lengths are easily achieved; maybe 20m. Special cable is available for LVDS is available with individual shielded twisted pairs, but we have not yet tested it. Also, factory-assembled cables with molded connectors are available. A disadvantage of the MDR connector is that currently it is apparently available only from 3M; we are currently looking for a second source. More information is available at http://www.mmm.com/interconnects/ (look for 'cable assemblies', 'MDR' and 'high frequency').