LVDS I/O Chip Propagation Skews

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At the informal Toronto VSI meeting the subject of propagation skews in LVDS line drivers and receivers was raised. The table from p.20 of [4] has been reproduced below with an extra column showing worst case within-chip and isothermal chip-chip skew. Comparable data for ECL 10k and 10kH devices has been added for comparison.

LVDS & ECL. Direct Parallel Port Devices

Transmitters						**Receivers**					
P/N	nTx	Vcc	Mbps	MHz	Δt_{max}	P/N	nRx	Vcc	Mbps	MHz	Δt_{max}
DS90C31B	4	5	128	64	1/3	DS90C32B	4	5	128	64	1.5/5
DS90C401	2	5	128	64	1/3	DS90C402	2	5	128	64	1.5/5
						DS90LV18A	1	3.3	256	128	-/1
						DS90LV28A	2	3.3	256	128	.5/1
DS90LV31A	4	3.3	256	128	.5/1	DS90LV32A	4	3.3	256	128	.5/1
DS90LV47A	4	3.3	256	128	.5/1	DS90LV48A	4	3.3	256	128	.5/1
SN65LVDS31	4	3.3	256	128	.3/.8	SN65LVDS32	4	3.3	256	128	.3/1
SN65LVDS3487	4	3.3	256	128	.3/.8	SN65LVDS3486	4	3.3	256	128	.3/1
SN65LVDS9638	2	3.3	256	128	.3/.8	SN65LVDS9637	2	3.3	256	128	.3/1
MC10124	4	-5.2	128	64	-/5.3	MC10125	4	-5.2	128	64	-/5.0
MC10H124	4	-5.2	256	128	-/2.1	MC10H125	4	-5.2	256	128	-/2.5

Δt_{max} is the maximum skew on_chip/between_chips, ns, over full Temp range.
Rated values over -40 to +85C for LVDS chips
t_{pd} Max-Min for MC10xx over -30 to +85C
t_{pd} Max-Min for MC10Hxx over 0 to +75C

References

[5] http://www.national.com/catalog/AnalogInterface.html
[23] http://www.ti.com/sc/docs/products/msp/intrface/index.htm {LVDS ...}
[40] VSI Port Technologies, 30/7/99
[41] MECL Device Data, DL122 Rev 4
