Updated Draft Proposal for
VLBI Standard Interface (VSI-H) Specification

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Introduction

The purpose of this document is to define a VLBI Hardware Standard Interface (VSI-H) to and from a VLBI 'Data Transmission System' (DTS) that allows hetergenous DTS's to be interfaced to both data-acquisition and correlator systems with a minimum of effort. The interface is defined to be compatible with traditional recording/playback systems, network data transmission and even direct-connect systems. It is designed to completely hide the detailed characteristics of the DTS and allow the data to be transferred from acquisition to correlator in a transparent manner.

A VLBI Standard *Software* Standard Interface (VSI-S) to accompany VSI-H is proposed but does not yet exist.

Intent of the Specification

The intent of the VSI-H specification is to define a standard electrical and timing interface, along with a control *philosophy*. In this sense, VSI-H is not intended to be completely 'plug and play', and will require at least some software customization in each case; the future adoption of a VSI-S specification will hopefully minimize the software customization as well. Nevertheless, the adoption of a standardized interface at the hardware level should help to relieve many of the existing incompatibilities that now exist between various VLBI data systems.

The VSI-H specification is primarily aimed at normal data-taking and data-correlation tasks commonplace to VLBI. However, some note will also be made to other related activities such as translation of tape media (i.e. tape copying) and parallel operation of multiple DTS's.

Structure of the VSI-H Specification

The VSI-H specification is structured as a *base* specification plus a set of optional extensions. It is intended that all VSI-H compliant systems will adhere at least to the base specification.

Assumptions on which VSI-H specification is based

The following assumptions were made in the development of the VSI-H specification:

- The DTS is fundamentally a receiver and transmitter of *bit streams.*
- The *meaning* of individual bit streams is not specified; normally, a bit-stream will be a stream of sign or magnitude bits associated with particular samples, but the actual meaning is to be mutually agreed upon between the data-acquisition system and the correlator.
- The received and transmitted bit-stream clock rates may be different (e.g. the playback rate of the correlator may be speeded-up or slowed-down), however all bit-

stream clock rates on acquisition must be the same, and all bit-stream clock rates on transmit must be the same.

- The data-acquisition time-tag of every bit in every bit-stream must be fully recoverable with no ambiguity.

Discussion

For the purposes of the VSI-H specification, the DTS is divided into two logical 'boxes', as indicated in Figure 1:

1. The 'Data Input Box' (DIB) receives the data-streams and low-level timing information from the data-acquisition system (DAS). Higher-level timing is generated within the DIB itself as will be discussed below.
2. The 'Data Output Box' (DOB) recreates the data-streams and low-level timing information as an exact replica of that received by the DIB. High-level timing information is managed in a simple interface between the DOB and the correlator such that precisely the correct data are provided at the DOB output.

There is no prohibition on the DIB and DOB residing in the same physical box, though economics sometimes dictates that they be separate boxes.

Operation of the 'Data Input Box' (DIB)

As shown in Figure 1, the DOB has the following interfaces:

1. Input signal from the DAS –
   a) A number of parallel bit streams.
   b) A CLOCK signal at the rate of the incoming bit streams and fully synchronous with the bit streams.
   c) A 1PPS tick which defines the data-bit taken on each second tick (lower-level time tags are inferred by counting bits from the 1PPS tick.

   Normally, the 1PPS and CLOCK signals will be synchronous and carried on the same connector. However, the 1PPS may also be provided from an external asynchronous source, such as a hydrogen maser; though allowed, this case may cause a 1-clock uncertainty in the time-tagging of the data.
2. Control Interface
   The DIB control interface is a 2-way communications interface, normally connected to a computer, which both monitors and controls the operation of the DIB. The DIB controller must be aware of 1PPS to the extent that certain messages can be reliably sent to the DIB between specific 1PPS pulses, and that certain messages can be reliably transmitted from the DIB between specific adjacent 1PPS pulses. In particular, there are two time critical messages:
   a) Set DOT clock to a specific time on the *next* 1PPS tick.
   b) Report DOT time immediately following a 1PPS tick.

The operation of the DIB is as follows:

The DAS is configured as necessary to provide the specified bit streams, along with the accompanying CLOCK and 1PPS tick; the DIB is likewise configured, through its control port, to accept the appropriate number of bit-streams at the specified bit-rate. The 1PPS

signal marks the data samples taken on the occurrence of the station second tick (presumably traceable to some station reference clock).

Through the DIB Control interface, the DOT is set to a specified integer second of time (presumably UTC) on a 1PPS tick. This is accomplished by sending a command to the DIB to set the DOT to a particular second of time at the *next* 1PPS. The DOT then keeps time by counting cycles of CLOCK, ignoring subsequent 1PPS signals unless asked to reset the DOT. The data are time-tagged as necessary by the DIB so that each bit in each bit-stream may be recovered with an unambiguous time-tag to the resolution of CLOCK.

The method the DIB uses to record data or to time-tag data is irrelevant to the VSI-H specification. And, of course, each type of DIB will have various control and configuration requirements which are outside the VSI-H specification and to which the data-acquisition software must adapt.

Note that if the DAS sample rate exceeds the maximum single-bit-stream data-rate, but not the maximum aggregate DTS rate, the DAS must have the responsibility to do the necessary parallel multiplexing before presentation to the DTS; the correlator, of course, must properly interpret the multiplexed data streams.

Operation of the 'Data Output Box'

As shown in Figure 1, the DOB has the following interfaces:

2. Output signals to the correlator –
   d) The reconstructed bit streams, accompanied by a common re-constructed clock (RCLOCK) and 1PPS tick (R1PPS). With the exception that these signals may be speeded up or slowed down relative to the rate which they entered the DIB, they are identical reproductions of those entering the DIB.[1]
   e) A single DATA_VALID signal indicating that the data emerging from the DOB is properly timed and valid.
   f) (Optional) Each reconstructed bit stream (RBSn) is accompanied by a 'data valid' signal (Vx) which indicates whether the data are believed to be valid or invalid on a bit-by-bit basis.

3. Input signals and control from the correlator –
   a) A control interface used to specify the setting of the Requested Observe Time (ROT), and to perform necessary configuration and control functions of the DOB. The ROT maintains the clock and generates a R1PPS ('reconstructed 1PPS') signal to which the reconstructed data must synchronize. The setting of the ROT is always to a specific time second (i.e. never a fractional second).
   b) A clock from the correlator (CORRCLOCK) which acts as a reference frequency to the DOB and from which RCLOCK ('reconstructed data clock') is derived. RCLOCK may be at a different rate than CLOCK (corresponding to a speedup or slowdown of the reconstructed data).

[1] Some DIB's (such as Mark III/IV recording systems) periodically replace small portions of the data with synchronization and time code information. In these cases, the DOB must flag such 'replacement data' as invalid.

c) A CORRTICK signal which sets the ROT clock in a manner similar to the way the 1PPS sets the DOT clock in the DIB. Typically, the CORRTICK signal will be periodic, with a period no shorter than ~1 sec of correlator wall clock time so that a computer control command can be comfortably issued between CORRTICK ticks. Because the correlator is assumed to have some degree of internal data buffering, the CORRTICK signal may be asynchronous with respect to CORRCLK within the limits of this buffering.

4. Control Interface

   The DOB control interface is a 2-way communications interface, normally connected to a computer, which both monitors and controls the operation of the DOB. The DOB controller must be aware of CORRTICK to the extent that certain messages can be reliably sent to the DOB between specific adjacent CORRTICK pulses, and that certain messages can be received reliably between specific adjacent CORRTICK pulses. In particular, there are two time critical messages:

   c) Set ROT clock to a specific time on the *next* CORRTICK.
   d) Report ROT time immediately following a CORRTICK.

Operation of the DOB is as follows:

Through its control port, the DOB is configured to reproduce the data streams. The DOB is informed of the number of CLOCK cycles per DOT second so that the DOB knows how many RCLOCK cycles correspond to a R1PPS tick period (and a ROT second). In the case of a tape recording, tape may have to be positioned to an approximate start-of-scan position.

Through the DOB Control interface, the ROT is set to a specified integer second of time on a CORRTICK tick; the precise method of accomplishing this is not part of the VSI-H specification. The ROT then keeps time by counting cycles of RCLOCK and generating the corresponding R1PPS signals.

On command, the DOB is responsible for constructing the reproduced bits-streams (RBSx's) properly aligned to ROT, RCLOCK and R1PPS. Since the DOB may not be able to create valid data until after some period of time (due to tape synchronization, etc.), bit streams are individually marked 'invalid' until the DOB is able to provide valid data. Data which are known or believed to be in error (due to tape reading errors, for example) are also marked 'invalid' so that they may be discarded in the correlation processing.[2]

Note that the reconstructed data stream from the DOB is, except possibly for the data rate and for playback errors or intentionally replaced data, *identical* to the data passed from the DAS to the DIB.

Normally, the CORRTICK pulses would be sent nearly synchronously to all DOB's, causing the DOB outputs all to be time aligned. This is satisfactory as long as the correlator has sufficient internal buffering to adjust the relative the data delays between stations before correlation. If limited internal correlator buffering is available, it may be

[2] In some cases, it may be desirable to inform the DOB of the start and ending times of a scan so that all data outside the scan-time may be marked invalid even though the DOB is reproducing accurate data.

possible to offset the CORRTICK pulses from one DOB to another to remove the bulk of the desired relative delay.

Since the correlator is presumed to have some internal buffering, R1PPS and RCLOCK need not be precisely aligned with CORRCLOCK and/or CORRTICK; the primary requirement is that the *relative* timing of R1PPS, RCLOCK and the data/validity lines is properly maintained.

For media translation (tape copying) purposes, the DOB must also have the capability of 'standalone playback' without the connection of CORRCLK or CORRTICK signals. In such case, the ROT clock will simply track the playback time on the tape. By using the DOB facility to transmit the ROT setting immediately following a R1PPS tick, a simple control computer can read the ROT and appropriately set the DOT clock in the DIB. Once ROT and DOT clocks are appropriately set, copying will take place with no further intervention.

Electrical and Timing Specifications

DIB data clock rates are 4, 8, 16, 32 and 64 MHz.

DOB data clock rates are also 4, 8, 16, 32 and 64 MHz, though slight deviations (a few percent, not yet specified) may be allowed.

All primary data and timing signals except 'Alternate 1PPS' and 'R1PPS Monitor' are ECL, which is well-established, easily available and reliable at 64 MHz clock rates. Use of the ECL10K logic family is recommended. The ECL timing specification is given in Figure 2 and Table 1.

Clock Rate (MHz)	tc(ns)	td(ns) transmit side	tw(ns)	tr(ns) 20-80%	tf(ns) 80-20%
4	250	125	125+/-3	5	5
8	125	62.5	62.5+/-3	5	5
16	62.5	31.25	31.25+/-3	5	5
32	31.25	15.625	15.625+/-3	5	5
64	15.625	7.8125	7.8125+/-3	3	5

Table 1: ECL Timing Specifications (see also Figure 2)

'Alternate 1PPS' and 'R1PPS' signals are standard TTL with active positive-going edges and no other significant timing specifications.

Control/Monitor Interfaces

Both the DIB and the DOB shall have *both* an Ethernet (preferably 10Base-T) *and* an RS-232 control interface. Some of the control and monitor functions, as discussed above, are quasi-real-time, in that control/monitor data must be reliably communicated between 1PPS pulses (in the DIB) or CORRTICK pulses (in the DOB) in order to proper set and monitor the DOT and ROT clocks.

The details of the communications messages and protocols is to be specified in the VSI-S document.

Physical Connections

DIB:

One D-sub 50 pin connector (male) for each set of 16 data streams with accompanying CLOCK and 1PPS signals (all ECL). Pin assignment is given in Table 2. Multiple parallel D-sub 50-pin connectors are allowed for systems with more than 16 data streams; in such case, each such connectors carries its own CLOCK and 1PPS signals which are appropriately timed for the data streams on that connector. Maximum timing skew 1PPS signals in parallel connectors is ???.

'Alternate 1PPS': 50-ohm BNC

Ethernet: 10Base-T

RS-232: Standard 9-pin wired as DCE. 1PPS should be reflected to pin ? as synchronizing timing signal.

DOB:

One D-sub 50 pin connector (female) for each set of 16 data streams with accompanying Data, RCLOCK, R1PPS and VALID signals. Pin assignment is compatible with DIB, except with addition of VALID signal. As is case with DIB, multiple parallel connectors are allowed for systems with more than 16 data streams.

'Monitor R1PPS': 50-ohm BNC

Ethernet: 10 Base-T

RS-232: Standard 9-in wired as DCE. R1PPS should be reflected to pin ? as a synchronizing timing signal.

Maximum cable length between DAS, DIB, DOB and correlator is 20 meters.

Notes and comments:

Media Translation (Tape Copying)

With the use of the VSI-H interfaces, data may be easily copied from one media to another in a straightforward manner. Data connectors are directly compatible. A simple program in a control computer can read time from the DOB RS-232 interface and transfer it to the DIB; note that this operation needs to be done only once at every time discontinuity on the tape.

Multiple Parallel DIB/DOB's

In the event that a single DTS is not able to handle the required aggregate data rate, multiple DTS's may be employed in parallel. In the case of the DIB, the DAS must be able to support multiple DIB's in parallel, each being supported as if it were standalone. Multiple parallel DOB's would normally be handled in the same way, though daisy-chaining of CORRTICK and CORRCLK could be acceptable depending on restrictions on allowable timing skew at the correlator input

Direct Connection

Note that the entire DTS can be just a set of straight-thru wires from the DAS to the correlator. In this case, the DOT and ROT are not required since presumably the correlator already is aware of the time. If the data are known to be valid, the validity lines are not needed.