Response to
"Draft Proposal for VLBI Standard Interface (VSI) Specification
3 February 1999"

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Comments and ***Proposed new text*** have been entered into an abridged form of the original.

Operation of the 'Data Input Box' (DIB)

As shown in Figure 1, the DIB has the following interfaces:

1. Interface to the data-acquisition system –
A number of bit-streams, accompanied by a common CLOCK,

Comment
CLOCK is defined to be at the bit stream rate. We note in passing that this contrasts with current practice in MkIV, VLBA and S2 systems where the accompanying clock is usually, if not always, 32MHz, regardless of the stream rate. There may be implications for backward compatibility here, except in the case of K4, and S2's 'FollowData' modes.

Operation of the 'Data Output Box'

As shown in Figure 1, the DOB also has the following interfaces:

1. Output signals to the correlator –
   a) The reconstructed bit streams, accompanied by a common re-constructed clock (RCLOCK) and 1PPS tick (R1PPS). With the exception that these signals may be speeded up or slowed down relative to the rate which they entered the DIB, they are identical reproductions of those entering the DIB.[1]
   b) Each reconstructed bit stream (RBSn) is accompanied by a 'data valid' signal (Vx) which indicates whether the data are believed to be valid or invalid on a bit-by-bit basis.

Comment
This validity spec doubles the number of high speed bit-streams, effectively doubling the size of the interface, and halving the capacity of any particular cable format. Given the current level of (non) usage of validity bits in some correlators the extra complexity may not be warranted. The use of a separate 'validity' cable between DOB and correlator should be considered. This would sensibly have the same format as the 'data' cable.

[1] Some DIB's (such as Mark III/IV recording systems, periodically replace small portions of the data with synchronisation and time code information. In these cases, the DOB must flag such 'replacement data' as invalid.

Electrical Specifications

All signals from DAS and to/from correlator are balanced ECL.

> **Comment**
> Continued use of balanced ECL line drivers and receivers is not obviously justified since real alternatives exist. For example LVDS provides equivalent performance with greatly reduced dissipation and cost, and runs off the same +5V or +3V power rails as the rest of the circuitry at each end of the cable.

Detailed timing specification TBD.
CORRCLOCK frequency – 32MHz (seems common among systems)

> **Comment**
> Given the state of contemporary technology the option of (at least) 64MHz could be considered here.

RCLOCK frequency – speedup desired when possible.

Physical Connections

DIB: Data, CLOCK, 1PPS – multi-pin connector(s) (TBD)
Control: RS-232(DB-9), GPIB and/or Ethernet (preferred)
Number of bit streams: 2^n (n at least =4)
Bit-stream data rates: 2^n Mhz (range of n TBD and is system specific)

DOB: Data, validity, RCLOCK, R1PPS – multi-pin connector (mating to DIB)

CORRCLOCK, CORRTICK – TTL 50Ω coax

> **Comment**
> CORRCLOCK & TICK could equally well be transmitted as low power balanced signals on a small format shielded multipair cable. Two more pairs could add full duplex serial communication if required.

Control: RS-232(DB-9), GPIB and/or Ethernet (preferred)

Notes: Input and output connectors and pin-outs should be compatible so that straight-

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Possibility to trade number of bit-streams with bit-stream rate?

System designers are encouraged to design systems which can trade the number of bit-streams with bit-stream-rate, so that the maximum aggregate rate of the DTS can be utilized as flexibly as possible.

Other notes and comments:

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4. If the DAS sample rate exceeds the maximum single-bit-stream data-rate, but not the maximum aggregate DTS rate, the DAS must have the responsibility to do the necessary parallel multiplexing before presentation to the DTS; the correlator, of course, must properly interpret the multiplexed data streams.

4.1 If the number of DAS data streams exceeds the maximum number of VSI single-bit-streams, without exceeding the maximum aggregate DTS rate, the DAS must have the responsibility to do the necessary multiplexing before presentation to the DTS; the correlator, of course, must properly interpret the multiplexed data streams.

Comment

While both 4. and proposed ***4.1*** are self-evident when their circumstances arise, they are also indicative of a general change in paradigm, namely that responsibility shifts to each DAS to conceal its own peculiarities behind a compact, generic interface. This then simplifies DTS interface requirements, in contrast to the cost and complexities of supporting an over-wide physical interface and a huge plethora of 'input modes' in order to accommodate all conceivable scenarios. There are flow on benefits in the correlator which in effect imitates the input modes in reverse.

4. and proposed ***4.1*** also suggest that DAS and correlator designers could benefit from a general convention on bit stream formatting. Likewise the formats in which a DTS will accept data when its aggregate rate is less than the installed VSI capacity, are of concern to all parties. These two conventions are one level removed from VSI which is essentially a physical interface description, but bear equally on the eventual interoperability of systems using it. This would seem to be an area for further discussion.
