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8 February, 2000

**TO:** VSI meeting attendees  
**FROM:** Alan Whitney  
**SUBJECT:** Summary of VSI-H meeting results

A two-day VSI meeting was held at Haystack Observatory 31 Jan – 1 Feb 2000 for the purpose of finalizing the VSI-H specification. The meeting attendees were:

Australia (by phone)

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The document ‘Updated Draft Proposal for VLBI Standard Interface (VSI-H) Specification’ dated 29 January 2000 served as the point of reference for the discussions at the meeting and is referred to in the summary below as the ‘current’ specification.

Following is a itemized summary of the main points of discussion and decisions arising from the meeting:

### Timing Signals

The ALT1PPS signal at the DIM input is modified from TTL to LVDS.

The DPSCLOCK and DPS1PPS signals are removed from the primary DOM signal interface. The signals ALTDPSCLK and ALTDPS1PPS are renamed to DPSCLOCK and DPS1PPS, respectively. This decision was brought about by Japanese design rules which prohibit bi-directional signals on the LVDS cables.

The DOM must include the capability to offset the delay of the reconstructed bit-streams with respect to the ROT clock by a specified bit offset, either positive or negative. This offset is controlled by a command issued through the control interface. The capability must exist to specify this offset for each R1PPS period, though this can be in the form of an initial offset at a specified R1PPS time tag plus an offset rate. When the reconstructed data are delay-offset in this manner, the R1PPS tick is also offset correspondingly. QVALID must be asserted logical false whenever the RBS are not synchronized according to the delay-offset command. More sophisticated delay models are, of course, allowed.

The minimum and maximum durations of various second ticks is given in the following table:

	<b>Min duration</b>	<b>Max duration</b>
1PPS	1 cycle of CLOCK	500 ns (inverse 2 MHz)
ALT1PPS	1 cycle of CLOCK	No specification
DPS1PPS	1 cycle of DPSCLOCK	500 ns
R1PPS	1 cycle of RCLOCK	500 ns

### Monitor

DOT1PPS and ROT1PPS signals will be 50-ohm TTL on BNC connectors.

The relationship between 1PPS and DOT1PPS is not specified in the VSI-H specification, but the expected timing relationship must be made known to the user. Ditto for ROT1PPS. For convenience, the DOT1PPS/ROT1PPS should be stretched for convenient scope viewing (but no hard specification).

Clarification: ROT1PPS occurs at *data* 1-pps rate. For example, if DOM data have 2x speedup, ROT1PPS has 2x speedup (that is, ROT1PPS would occur at a rate of 2pps in that case).

### Connectors and Cable

The LVDS signals ALT1PPS, DPSCLOCK and DPS1PPS will all be defined on a single 14-pin LVDS connector. If the DIM/DOM are in a single box, all three of these signals will be present. If the DIM and DOM are in separate boxes, only the respectively relevant signals will be present (or will be used).

LVDS cable specs need to be included (Dick Ferris has agreed to give this a go.):

- cable rise time spec
- pair-to-pair max skew
- characteristic impedance (100-110-ohm)

LVDS devices must be TIA/EIA-644 standard.

LVDS max cable length is a function of clock speed. From manufacturer's data, it appears 20m cable length is acceptable even at clock rate of 128 MHz.

Suggestion was made to put all unused pins on 80-pin connectors at one end. This would allow a new function to use a contiguous set of pins.

All pins on LVDS connectors must be driven. 'Reserved' signals must have transmitter and receiver attached and active; transmitter will be held at active '0' or '1'. All signals on each LVDS cable must flow in the same direction.

No LVDS-connector pins will be assigned to ground. Ground is normally carried through on the cable shield.

The RS-232 control interface will use an RJ-45 connector on the DIM and DOM.

The Ethernet control interface will be 10Base-T or 10/100Base-T (RJ-45 connector).

*Signal selection and switching*

Any subset of 2<sup>n</sup> DIM input bit-streams may selected to be 'active'.

The VSI-H specification will be functional only and specify that 'any active DIM input bit-stream must be mappable to any DOM output bit-stream. The VSI-H will not specify how this is to be accomplished. The functional block diagram may show a crossbar switch indicated as 'for illustrative purposes only'.

*Clocking*

Long discussion on 'fixed' vs 'variable' CLOCK signal; probably most difficult issue to settle. Agreement was finally reached on a 'compromise' which might be called 'variable fixed' CLOCK/DPSCLOCK.

I propose to define a new term, *bit-stream information rate (BSIR)*, which describes that actual information rate of a data bit-stream that is passed into the DIM or out of the DOM; BSIR must be <= *bit-stream clock rate (BSCR)*. This is an important distinction since, for example, the DAS may provide the DIM with data at a constant BSCR, but the DIM is set to sample this data only at the BSIR, which may be at a lower rate.

The following table defines the allowed set of clocks and BSIR's for the DIM and DOM:

CLOCK/ RCLOCK (MHz)	BSIR <sub>n</sub> /RBSIR <sub>n</sub> (Mbps)						
	2	4	8	16	32	64	128
2	Y						
4	Y	Y					
8	Y	Y	Y				
16	Y	Y	Y	Y			
32	Y	Y	Y	Y	Y		

<b>64</b>	opt	opt	Y	Y	Y	Y	Y
<b>128</b>	opt	opt	opt	Y	Y	Y	Y

Notes:

1. 'Y' indicates required
2. 'opt' indicates optional
3. CLOCK frequencies of 64 and 128 MHz are extensions to the VSI-H standard.

The following table defines the allowed set of DPSCLOCK vs. RCLOCK rates for the DOM:

<b>DPSCLOCK (MHz)</b>	<b>RCLOCK (MHz)</b>						
	<b>2</b>	<b>4</b>	<b>8</b>	<b>16</b>	<b>32</b>	<b>64</b>	<b>128</b>
<b>2</b>	Y						
<b>4</b>	Y	Y					
<b>8</b>	Y	Y	Y				
<b>16</b>	Y	Y	Y	Y			
<b>32</b>	Y	Y	Y	Y	Y		
<b>64</b>	opt	opt	Y	Y	Y	Y	Y
<b>128</b>	opt	opt	opt	Y	Y	Y	Y

Notes:

4. 'Y' indicates required
5. 'opt' indicates optional
6. DPSCLOCK frequencies of 64 and 128 MHz are extensions to the VSI-H standard.

The timing diagram of Figure 2 needs to be expanded to show timing for several different clock frequencies.

Note that it may be necessary to reset all or various parts of a DIM/DOM after a change in CLOCK/DPSCLOCK frequency.

#### *Test Vector*

Inclusion of the specified test-vector capabilities is a VSI-H base specification (though there is some difference in recollection on this point – maybe someone can help).

The TV specification is relevant only for tests from DAS to DIM, DOM to DPS, and DOM to DIM (tape copying). The specification is mute with respect to tests between the DIM and DOM since these tests fall entirely within the DTS and are not visible to the user.

TVG timing needs to be more completely specified.

Suggested TVG implementation needs some additional work to meet various combinations of clock and data rates (action item for Wayne).

### *Other*

A new PVALID signal is defined at the primary DIM input connector, which may be used to mark valid data to the DIM; PVALID may optionally be transmitted to the DOM, where it can be “and’ed” with a DOM-internally-generated ‘VALID’ signal (which has the same definition as VALID in the 29 Jan document) to create QVALID, which replaces current VALID at the output of the DOM.

More examples of the use of PDATA and QDATA would be useful.

For some DOM standalone applications, such as tape copying, the DOM should have a mechanism to produce all relevant reconstructed signals (R1PPS, RCLOCK, RBS<sub>n</sub>, plus QVALID/QDATA as relevant or needed) without the need for DPSCLOCK/DPS1PPS signals.

Multiple DIM/DOM capability needs better explanation.

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The following are my further thoughts on a couple of matters, and I solicit feedback:

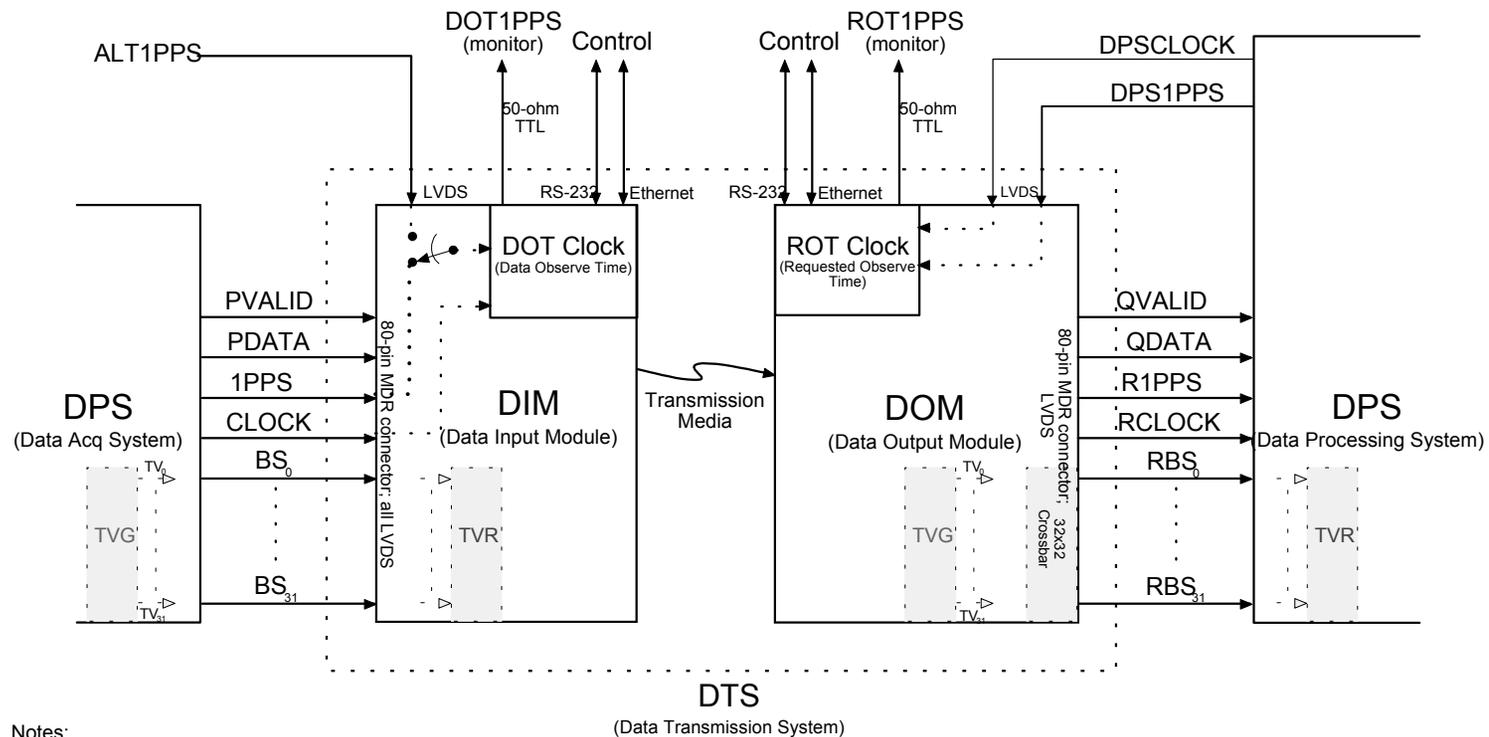
#### *Levels of VSI-H Compliance*

Perhaps two levels of VSI-H compliance can be specified to clarify the compliance situation:

1. DTS’s which fully comply with the VSI-H standard will be declared to be ‘Level A’ compliant.
2. DTS’s which are compliant except for one or more of the following items are said to be ‘Level B’ compliant:
  - Support for fewer than 32 bit streams
  - Incomplete signal-switching active-signal-selection capability
  - Incomplete support of all CLOCK frequencies
  - Incomplete test-vector capability

#### *Validity per bit-stream*

I propose that, for the present, we remove the DOM-generated validity-signal per bit-stream option currently in the spec. Rather than use a separate parallel connector for this purpose, it has been suggested by Hans Hinteregger at Haystack that a more sensible method of indicating DOM-generated validity on a per-bit-stream basis might be to use a ‘bi-phase code’ on the RBS output bit streams themselves. This works by using the second half of each RBS bit cell to indicate the validity state of that bit, so that the negative-going transition of RCLOCK samples the validity state of each bit cell of every RBS<sub>n</sub>; this effectively means that the RBS data rate is doubled. Coding can be chosen so that a *change* of level in the second half of the bit cell signifies invalidation; this coding means that a bit stream without per-bit-validation is identical to a fully-valid bit stream with per-bit-validation. A DPS may choose to use this information or not, as he chooses. Note that this would have no impact on the base VSI-H specification. This bi-phase coding scheme is apparently quite common in commercial applications. Please note that we are talking about only *DOM-generated* validity signals; these validity states are *not* transmitted directly from the DIM to DOM. The conditions used to control the per-bit-stream validation signals may presumably be specified by the user and is may be dependent on the details of the DTS system.



Notes:

1. Shaded items are for illustrative purposes only.
2. PVALID is optionally transmitted from DIM to DOM.
3. PDATA is optionally transmitted from DIM to DOM.
4. This diagram does not show all functions and options -- see specification details.

Figure 1: VSI-H Functional Block Diagram

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